New High Performance Low Power Carry Look Ahead Adder With Reduce Ground Bounce Noise Using MTCMOS Technique

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Abstract: In this pepper we have designed a carry look adder circuit using CMOS technique, the low power and reduce Ground Bounce noise Carry look Ahead Adder has been proposed. A carry look ahead adder improves the speed by reducing the time required to solve carry bits. Carry-look ahead adder is a major functional block in arithmetic logic unit due to its high speed operation. The arithmetic logic unit has been widely used in microprocessor systems and mostly in processing modules of embedded systems. As the speed of the circuit increases the most important unwanted parameter exhibited by the circuits is ground bounce noise. In this paper, we have proposed a modified Carry look Ahead Adder based on using multi-threshold CMOS technique .Here we use MTCMOS technique to evaluate standby leakage current, power and ground bounce noise. All the simulation in this paper has been carried out using Empyrean Aether" tool at 180nm technology at various voltage and temperatures.

Keywords: Ground bounce noise, Leakage power, Multi-threshold CMOS, Carry looks ahead adder.

I. INTRODUCTION

In the past major challenges for VLSI designer to reduce the area of chip. One of the most important issues in VLSI design is standby leakage current with continuous down scaling in advanced CMOS technology. The leakage current contributes 49-64% in active power [1] [2] of digital circuit. It affects active power; standby power and performance of digital circuits because leakage strongly depends on process variations, increase in number of transistor and technology scaling. In this paper, we have proposed new Carry look Ahead Adder with low power and fixation identification from raw eye motion signals. Reduce ground bounce noise based on conventional Carry look ahead adder. Carry look ahead adder .In recent years, various logic styles have been proposed to implement low power adder with reduced ground bounce noise.[3] [4]. The main idea behind this paper aims at design, analysis and improvement of power efficiency and ground bounce noise reduction of the Carry look Ahead adder at 180nm technology. The power reduction in any logic circuit cannot be achieved with trading off performance because it can make harder to reduce leakage during run time operation. We have seen several techniques proposed to reduce leakage power [5]. One of the most important technique Multithreshold (MTCMOS) also known as power gating technique is used for reducing the leakage current and standby leakage power when device is in idle mode and to

improve the performance of device in active mode. The main idea behind this technique is to turnoff device in sleep mode and cut off leakage path provides a reduced leakage with improved power performance and reduction in ground bounce noise with proposed novel technique with improved stacking and power gating[6].

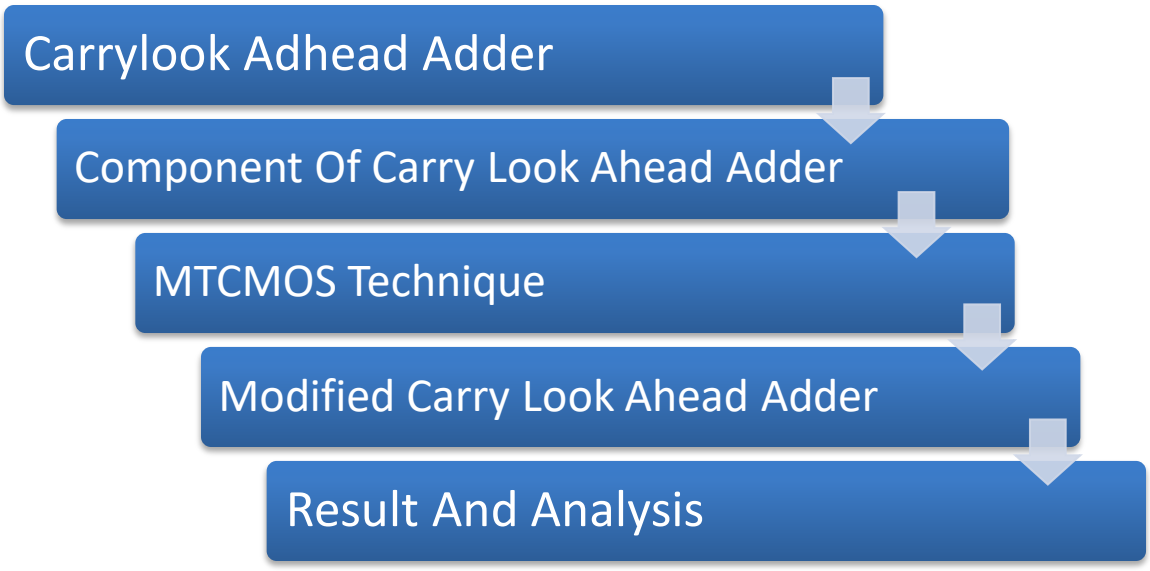

Figure1. Schematic diagram of proposed methodology

II. PROPOSED METHODOLOGY

We have proposed a modified Carry look Ahead Adder based on using multi-threshold CMOS technique .Here we use MTCMOS technique to evaluate standby leakage current, power and ground bounce noise.

A. Carry Look Ahead Adder:

A Carry Look ahead adder is a fast parallel adder as it reduces the propagation delay by more complex hardware; there are faster ways to add two binary numbers by using carry look ahead adders[7]. They work by creating two signals P and G known to be **Carry Propagator** and **Carry Generator**. The signal from input carry C_{in} to output carry Cout requires an AND gate and an OR gate. Carry Look Ahead Adder Generate two Signals P (Carry Propagator) and other G (Carry Generate) The corresponding Boolean expressions are given here to construct a carry look ahead adder. In the carry-look ahead circuit we need to generate the two signals carry propagator (P) and carry generator (G).

$$Pi = Ai \oplus Bi \dots\dots\dots\dots\dots\dots\dots\dots\dots (1)$$

$$Gi = Ai \cdot Bi \dots\dots\dots\dots\dots\dots\dots\dots\dots (2)$$

The output sum and carry can be expressed as

$$Sum = Pi \oplus Ci \dots\dots\dots\dots\dots\dots\dots\dots (3)$$

$$Ci + 1 = Gi + (Pi \cdot Ci) \dots\dots\dots\dots\dots\dots\dots\dots\dots (4)$$

Having these we could design the circuit. We can now write the Boolean function for the carry output of each stage and substitute for each Ci its value from the previous equations:

$$C1 = G0 + P0 \cdot C0 \dots\dots\dots\dots\dots\dots\dots\dots\dots (5)$$

$$C2 = G1 + P1 \cdot C1 = G1 + P1 \cdot G0 + P1 \cdot P0 \cdot C0 \ldots\ldots\ldots\ldots\ldots\ldots\ldots (6)$$

$$C3 = G2 + P2 \cdot C2 = G2P2 \cdot G1 + P2 \cdot P1 \cdot G0 + P2 \cdot P1 \cdot C0 \ldots\ldots\ldots (7)$$

$$C4 = G3 + P3 \cdot C3 = G3P3 \cdot G2P3 \cdot P2 \cdot G1 + P3 \cdot P2 \cdot P1 \cdot G0 + P3 \cdot P2 \cdot P1 \cdot C0 \ldots\ldots\ldots (8)$$

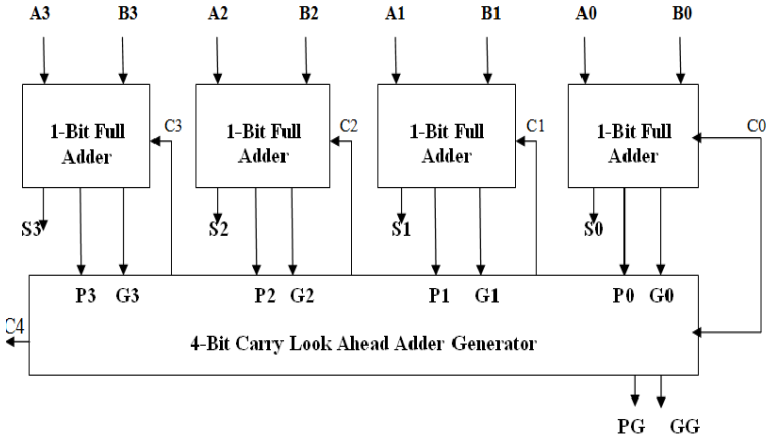

Figure1. Carry Look Ahead Adder

B. COMPONENT OF CARRY LOOK AHEAD ADDER

- **28T FULL ADDER**

One way to implement the full adder circuit is to take the logic equation (9) and equation (10) and translate them directly into complementary CMOS circuit. Some logic manipulations can help to reduce the transistor count[10]. For instance, it is advantageous to share some logic between the sum and carry –generation sub circuits, as long as this does not slow down the carry generation, which is the most critical part as stated previously[11]

The following is an example of such as reorganized equation set

$$CARRY = A \cdot B + B \cdot Cin + A \cdot Cin \ldots\ldots\ldots\ldots\ldots\ldots\ldots (9)$$

$$Sum = A \cdot B \cdot Cin + CARRY(A + B + Cin) \ldots\ldots\ldots\ldots\ldots (10)$$

The equivalence with the original equations is easily verified. The corresponding adder design, using complementary static CMOS, is shown in figure 2 and the gate level implementation is shown in figure 2. It requires 28 transistors. In addition to consuming a large area, this circuit is slow [12][13]. Here

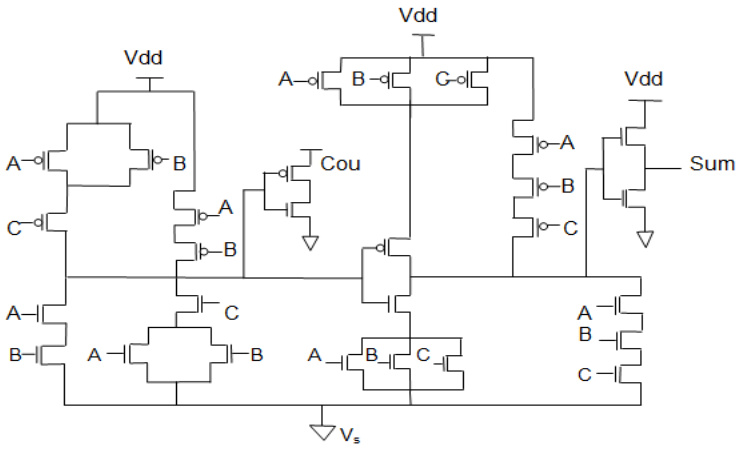

Figure 2. 28 T Full Adder

- **AND GATE:** Conventional AND Gate is the combination of PMOS and NMOS [14]. The circuit shows the realization of CMOS AND gate.

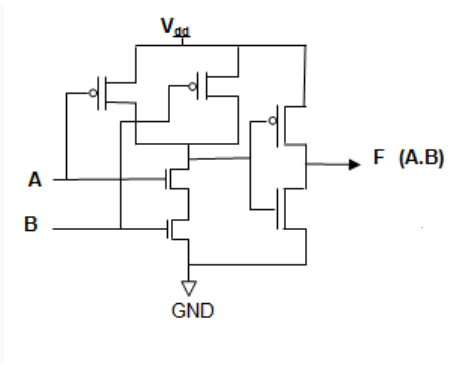

Figure 3 Conventional AND Gate

- **OR GATE:** Conventional OR Gate is the combination of PMOS and NMOS. The circuit shows the realization of CMOS OR gate.

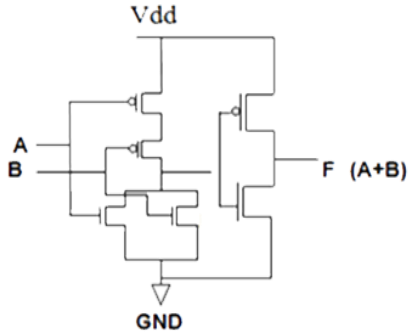

Figure 4 Conventional OR Gate

C. MTCMOS TECHNIQUE

The power gating circuit could work in three different modes:

- Active mode, in which the sleep transistor is on and the circuit function normally.
- Sleep mode, in which the sleep transistor is shut-off and the leakage current of entire circuit is suppressed. The sleep transistor is switched 'off' to block leakage paths between the power and ground rails which could otherwise steadily draw power even during standby.
- Transition mode, in which the sleep transistor is turned on and the circuit goes from sleep to active [15]. Ground Bounce effect usually occurs in transition mode.
- In the active mode, sleep transistors are turned on and the logic consisting of low *VT* transistors can operate with high speed and low switching power dissipation. When the circuit is in sleep mode the high *VT* transistors are turned off cause nag isolation of low *VT* transistor from supply voltage and ground thereby reducing sub-threshold leakage current.

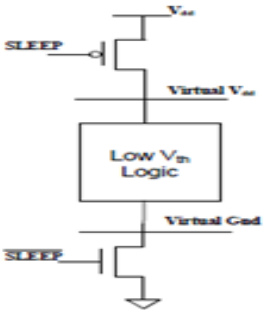

Figure.5 Logic Circuit MTCMOS Technique.

D. MODIFIED CARRY LOOK AHEAD ADDER

We have proposed Carry look ahead adder with MTCMOS technique is implemented where a sleep transistor is added between actual ground rail and circuit ground. The device is turned off during sleep mode to cut-off the leakage path. [16] The comparison of active power, standby leakage power is done and it's observed that power is greatly reduced as we move from conventional CMOS Carry look ahead adder to Modified Carry Look Ahead Adder.

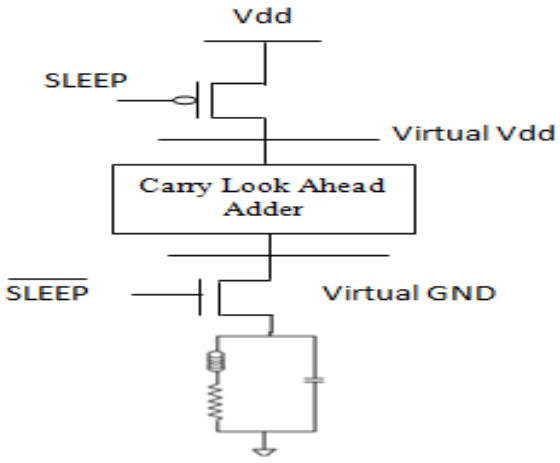

Figure.5 2. Modifed Carry look Ahead Adder

III. EXPERIMENTAL SETUP & SOFTWARE

We have used Empyrean Aether" tool at 180nm technology at various voltage and temperatures

IV. RESULTS AND ANALYSIS

In this section, we have performed simulation of our conventional carry look ahead adder (adder with MTCMOS) on Empyrean Aether Tool at MTCMOS Technology

- **ACTIVE POWER**

At the time of operating the power is dissipated by the circuit is known as active power. Active power includes both static power and dynamic power of the circuit. Here we have calculated the active power of the circuit at various voltage and temperature. The Active power consumption of CMOS circuit [17] is consumed by the following equation.

$$Pactive = Pdynamic + Pstatic \dots\dots\dots\dots\dots\dots\dots (11)$$

$$Pavg = Pswitching + Pshort - circuit + Pleakage \dots\dots\dots\dots\dots\dots\dots (12)$$

$$P = (\alpha 0 \rightarrow 1CL \cdot V^2dd \cdot fclk) + (Isc \cdot Vdd) + (Ileakage \cdot Vdd) \dots\dots (13)$$

The first term represents the switching component of power, where C_L is the load capacitance, f_{clk} is the clock frequency and $\alpha_{0->1}$is the probability that a power consuming transition occurs (the activity factor). The second term is due to the direct-path short circuit current, I_{sc}, which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground, finally, leakage current, $I_{leakage}$. As shown the table 1 in the case of modified Carry look ahead adder with stacking power gating active power is reduced compared to conventional Carry look ahead adder. 64 % at voltage 1.8 V and temperature 27 ^{o}C .

TABLE 1 ACTIVE POWER DISSIPATION OF CARRY LOOK AHEAD ADDER

Circuit	Con. Carry Look Ahead Adder		Modified Carry Look Ahead	
Supply and Temperature	1.8 V	27 ^{o}C	1.8 V	27 ^{o}C
Active	108.7	108.7	45.23	45.23

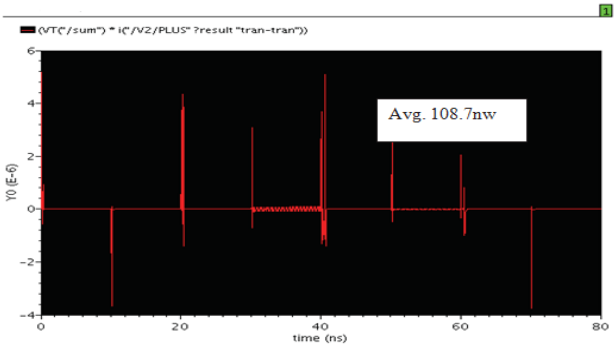

Figure 7 (a) Active power of conventional Carry Look Ahead Adder

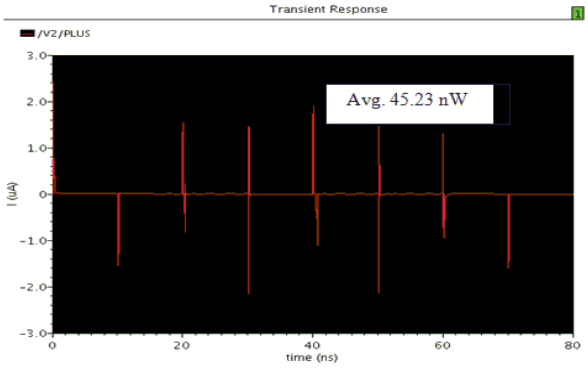

Figure 7 (b) Active power of modified Carry Look Ahead Adder

- **STANDBY LEAKAGE CURRENT**

The stand by leakage is obtained when the circuit in idle mode. Here we connect the sleep transistor to the pull down network of Carry look ahead adder circuit and ground of the circuit. When we measuring the leakage current in MTCMOS Power gating then the both transistors are off [18]. The basic equation of stand by leakage is

$$Leak = Isub + Iox \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (14)$$

Where, I_{sub} = Sub threshold leakage current, I_{ox} = Gate oxide current. Stand by leakage current is measured by at 1.8V and 27ºC. It is greatly reduced almost 49 % in modified Carry look ahead adder with MTCMOS power gating. The table 2.(a) shows the leakage current at various voltages and various temperatures.

TABLE 2 (A) STANDBY LEAKAGE CURRENT AND LEAKAGE POWER DUE TO VARIOUS VOLTAGES

Volt. (v)	Leakage current		Leakage power	
	Conventional Carry look ahead (nA)	Modified Carry look ahead (pA)	Conventional Carry look ahead (mW)	Modified Carry look ahead (nW)
1.6	91.80	46.53	29.23	100.89
1.8	158.15	78.37	72.76	113.15
2.0	230.50	156.20	143.59	133.23
2.2	281.70	218.48	290.89	143.69
2.4	343.50	399.18	345.50	223.50

TABLE 2 (B) STANDBY LEAKAGE CURRENT AND LEAKAGE POWER DUE TO VARIOUS TEMPERATURES

	Leakage current	Leakage power

Temp. 0_C	Conventional Carrylook ahead adder (nA)	Modified Carry look ahead adder (pA)	Conventional Carry look ahead adder (m W)	Modified Carry look ahead adder (n W)
27	157.18	78.36	72.76	113.19
47	160.70	139.20	76.80	253.69
67	162.70	248.50	79.68	387.70
87	165.80	317.30	80.55	455.36
107	193.50	423.80	90.70	573.43s

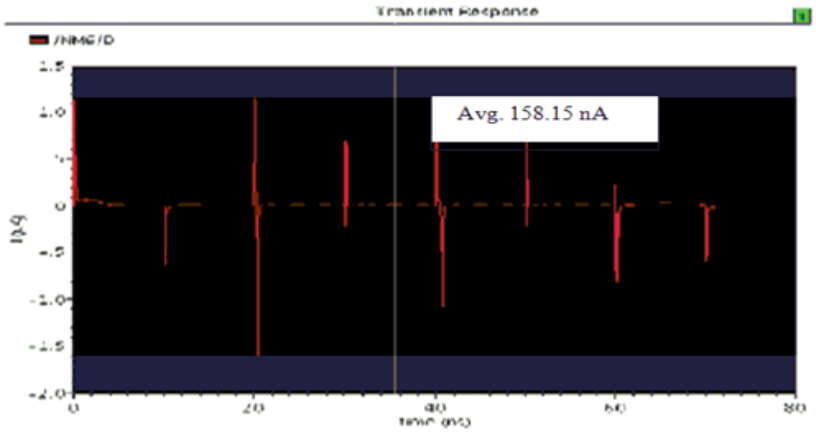

Figure 8 (a) Leakage current of conventional Carry Look Ahead Adder

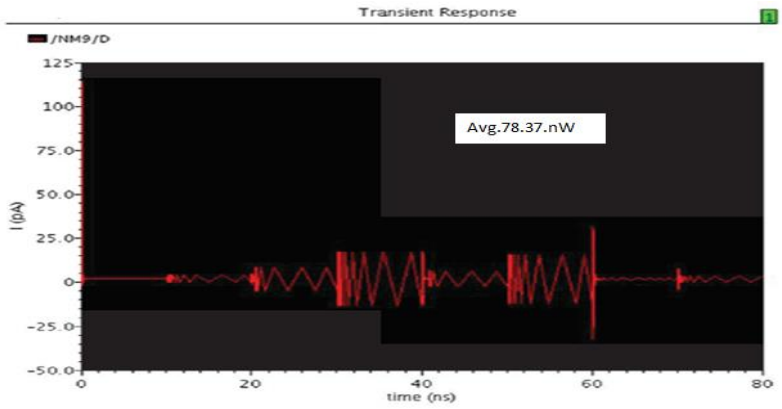

Figure 8 (b) Leakage current of modified Carry Look Ahead Adder

- **LEAKAGE POWER**

The stand by leakage power is measured at the time of idle mode. Here measured the leakage power when the sleep transistor is off. Basically the stand by leakage power is the product of the leakage current and supply voltage [19].The basic equation of leakage power is

$$Pleak = Ileak \cdot Vdd \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (15)$$

The Table 2 (a) and Table 2 (b) shows leakage power is reduced in various voltages and temperatures after applying stacking power gating.

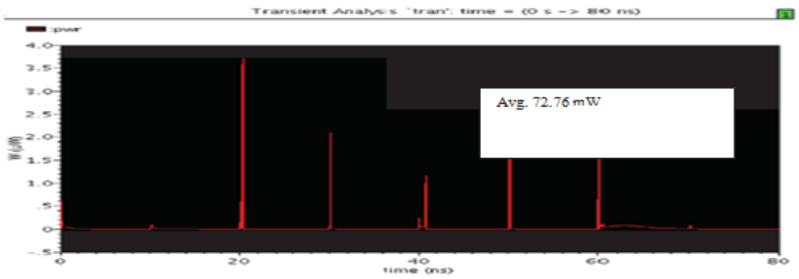

Figure 9(a). Leakage power wave of conventional Carry look ahead adder

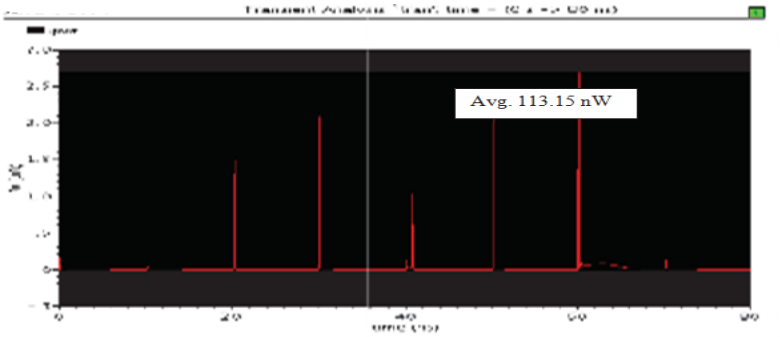

Figure 9(b). Leakage power wave form of modified carry look ahead adder

- **GROUND BOUNCE NOISE**

During the active mode of the circuit an instant current pass from sleep transistor, which is saturation region and causes a sudden rush of the current. Elsewhere , because of self inductance of the off- chip bonding wires and parasitic inductance on chip power rails, result voltage function in the circuit depends on input/ output buffers and internal circuitry. The noise depends on the voltage. The ground bounce noise mode is in Fig 10. [20][21].

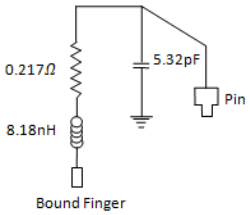

Figure.10: DIP-40 Package Pin Ground Bounce Noise mode

• Inductance L = 8.18 nH

• Resistance R = 0.217 Ω

• Capacitance C = 5.32 pF

The following wave form is showing ground bounce noise of conventional Carry look ahead Adder and modified Carry look ahead Adder.

TABLE 3.GROUND BOUNCE NOISE FOR CARRY LOOK AHEAD ADDER

Voltage (V)	Ground Bounce Noise (nV)		Temp ^{0}C	Ground Bounce Noise (nV)	
	Conv.	Modified		conv	Modified
1.6	65.30	18.34	27	63.63	41.85
1.8	63.80	40.75	47	66.42	33.26
2.0	96.40	64.41	67	69.33	44.31
2.2	125.90	89.23	87	74.66	53.32
2.4	157.14	115.90	107	80.40	63.92

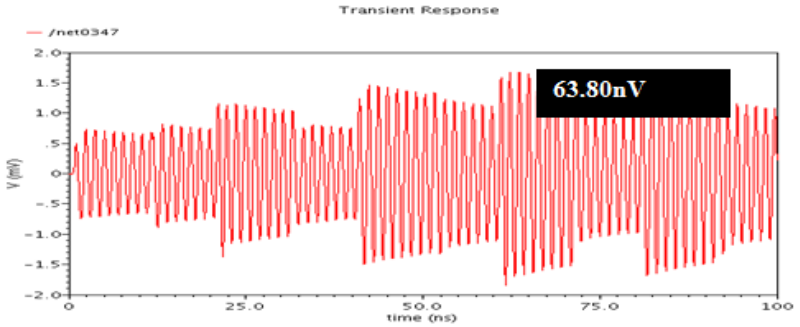

Figure 11 (a) Ground Bounce Noise of Conventional Carry look ahead Adder

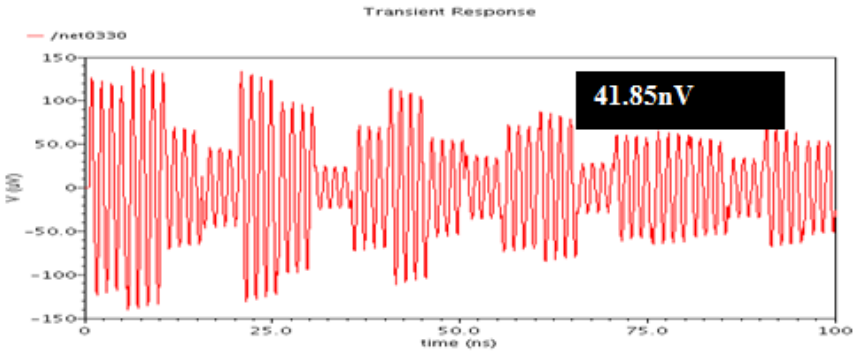

Figure 11.(b) Ground Bounce Noise of modified Carry look ahead Adder

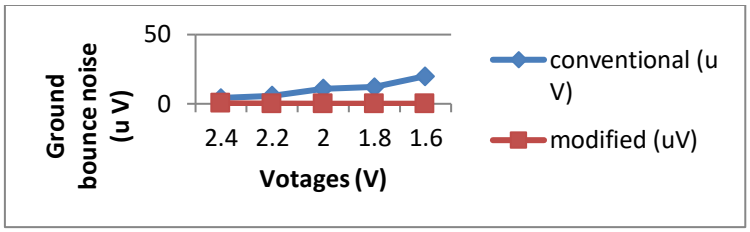

Figure 12. (a) Ground Bounce Noise graph of Carry look ahead Adder at various voltages

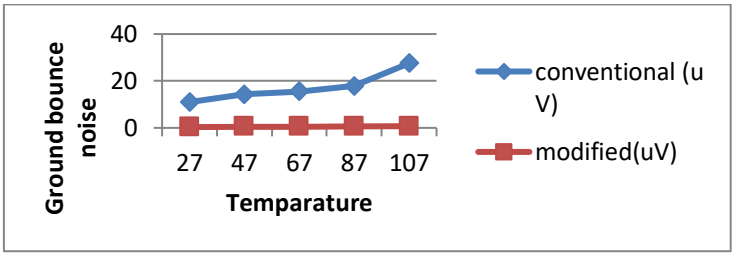

Figure 12 (b): Ground Bounce Noise graph of Carry look ahead Adder at various Temperatures

As shown in the table, the ground bounce noise is reduced up to 65 % in to various voltage and temperature

V. CONCLUSION

In this Paper Carry look ahead adder with MTCMOS technique is implemented where a sleep transistor is added between actual ground rail and circuit ground. The device is turned off during sleep mode to cut-off the leakage path. The comparison of active power, standby leakage power is done and it's observed that power is greatly reduced as we move from conventional CMOS Carry look ahead adder to Modified Carry Look Ahead Adder. The leakage current is up to 49% and leakage power up to 69 %. The ground bounce noise is reduced to up to 65% and active power is reduced up to 64%. The proposed modified Carry Look Ahead adder is operated at various voltages and various temperatures.

ACKNOWLEDGEMENT

I would like to thank my mentor Mr. Raghvendra Singh Assistant Professor for introducing me to this exciting area of New High Performance Low Power Carry Look Ahead Adder With Reduce Ground Bounce Noise Using MTCMOS Technique. . I would like to thank Dr. Vivek Srivastva Dean, Faculty of Engineering and Technology, for the valuable suggestions time to time. I would also like to thank Mr. Samir Mishra, Assistant Professor, HOD Electronics and Communication Engineering, for the valuable suggestions time to time in my programming & simulation work Authors would also like to Manish Kumar, Md. Anwar Hussain, Sajal K.Paul thanks to This work is supported by Rama University Uttar Pradesh, Kanpur. for providing valuable suggestion in MTCMOS Technique.

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