Design and Analysis of Parallel Self Time 4 Bit Adder with Reduce Ground Bounce noise

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Abstract:-In this Paper, A parallel Self Time 4 Bit Adder used with low power & reduce Ground Bounce noise. It uses recursive method for performing multi bit binary adder. The operation is parallel for those bits that do not need any carry chain propogation. The operation is parallel for those bits that do not any carry chain propogation. This design attains good performance without any special speed up circuitry. This design attains good performance without any special speed up circuitry. This adders have the capacitor to run faster than all other circuit design. This Adder uses Half adder along with Multiplexer requiring minimal inter connections. The speed of circuit is increases the unwanted ground noise. in this paper multi-threshold CMOS Techniques used with 4 bit A parallel self time adder. so this paper shall calculate leakage current, Power and ground Bounce noise. The simulations this paper have been performed using cadence "empyrean aether tool" and SPECTRE simulator at 180 nm technology.

Keywords: Multi-threshold CMOS, Stack transistor, Ground Bounce noise, Parallel Self Time Adder, Stand by leakage power.

Introduction:

The Scaling down techniques the major issues is stand by leakage current in advanced CMOS technology. The leakage current in advanced CMOS Technology. The leakage current is 50-60% in Active Power [1][13]. we proceed process variation the leakage strongly increases, increase in no of transistor and technology Scaling. we have proposed new 4 bit parallel self time adder by reduce ground bounce noise and low power. The parallel self time adder is fundamental unit which performing arithmetic and multiplier ,comparator operation and parity checker as well as digital signal processing.[12][17][18].The main goal of this paper is to implement the adder to reduce power and increase speed.[16][19].

During run time operation, It can make harder to reduce leakage. so the power reduction in any logic circuit can not be achieved with trade off. [20]

There many several technology proposed to reduce leakage.[20].The main idea this technique, The device in sleep mode during turn off and It is improved power performance by cut off leakage path provides reduced leakage.[23][24].It is ideal Technique to improve power gating. The MT-CMOS Technique is reducing leakage current and leakage current leakage stand by power.

Asynchronous circuits:

An asynchronous circuit or self-timed circuit is a sequential digital logic circuit which is not governed by a clock circuit or global clock signal. Instead they often use signals that indicate completion Of instructions and operations, specified by simple data transfer protocols. This type is contrasted with a synchronous circuit in which changes to the signal values in the circuit are triggered by repetitive pulses called a clock signal. Most digital devices today use synchronous circuits. However asynchronous circuits have the potential to be faster, and may also have advantages in lower power consumption, Asynchronous circuits are an active area of research in digital logic design. In asynchronous circuits, there is no clock. asynchronous circuits can be faster than synchronous circuits[2][4][6].

Half-Adder:

The half adder adds two single binary digits A and B. It has two outputs, sum (S) and carry (C). The carry signal represents an overflow into the next digit of a multi-digit The value of the sum is 2C + S. in corporate s for XOR gate and c for AND gate. The two half adder makes one full adder. The half adder adds two input bits and generates a carry and sum, which are the two outputs of a half adder. The input variables of a half adder are called the augends and addend bits. The output variables are the sum and carry [2].

Mux:

In electronics, a multiplexer is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2n inputs has "n" select lines, which are used to select which input line to send to the output. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A multiplexer is also called a data selector. An electronic multiplexer can be considered as a multiple-input, single-output switch The schematic on the right shows a 2-to-1 multiplexer on the left and an equivalent switch on the right. The wire connects the desired input to the output. The basic function of a multiplexer: combining multiple inputs into a single data stream.

Binary Addition:

In digital electronics. A binary number is another name is base-2 numeral system which represent two value either 0 or 1.The radix is base 2 system is 2. Binary system is used all computer &computer based device [2].

PROPOSED ADDER APPROACH:

The design of PASTA is regular and uses half-adders (HAs) along with multiplexers requiring minimal interconnections. The Adder approach in this circuitry is independent carry chain block is parallel manner. The digital circuitry design style is governed by CMOS.This implement of the circuit on the integrated circuit. The logic families are great power so the CMOS circuitry is use. The most of integrated circuit are designing CMOS processes [15].

Architecture of PASTA:

The general architecture of the adder is shown in fig.1.1.The selection i/p multiplexer corresponds to req-hand shake signal and will be a single 0 to 1 transition denoted by SEL.
This adder will initially select the actual operands during SEL=0 and will switch to feedback/carry paths for subsequent iterations using SEL=1. The feedback path from the HAs enables the multiple iterations to continue until the completion when all carry signals will assume zero values [15].

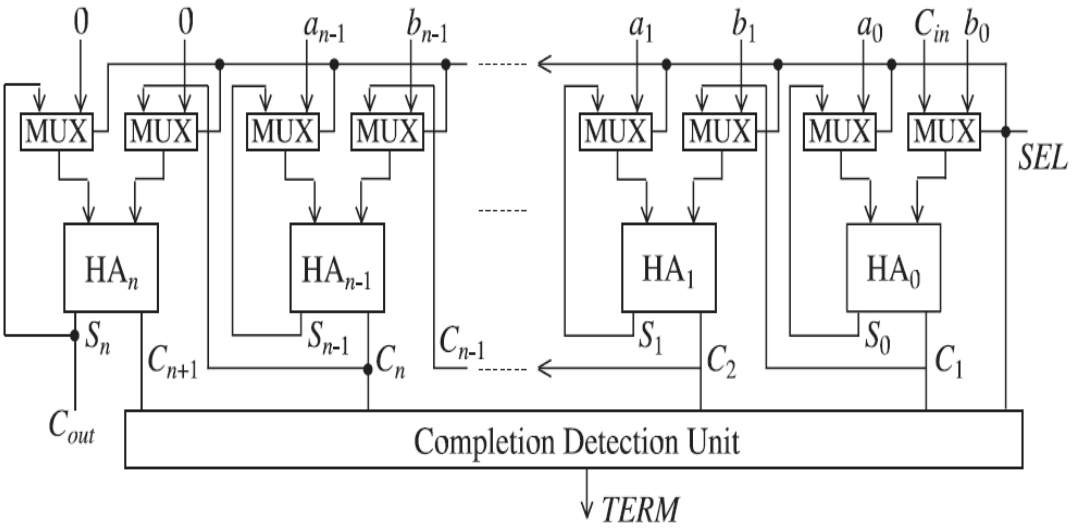


FIG.1.1 GENERAL BLOCK DIAGRAM OF PASTA

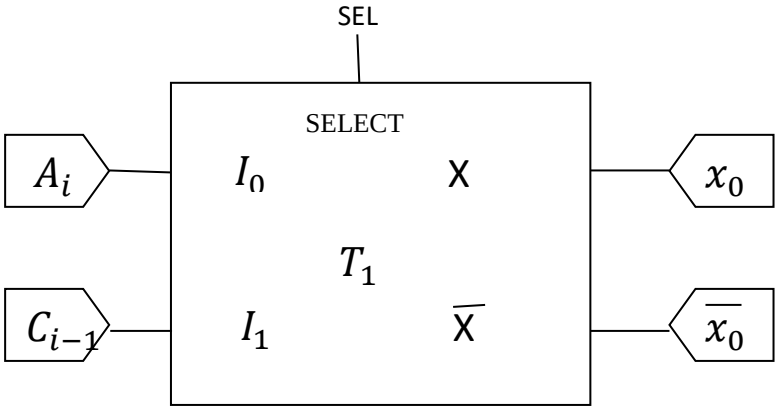


FIG.1.2

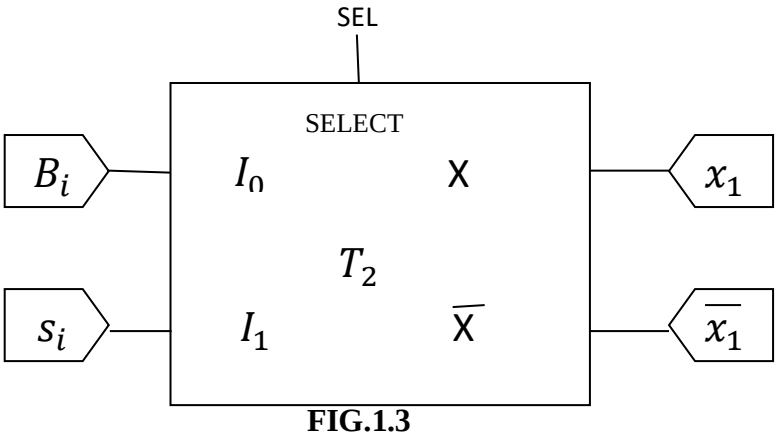


FIG.1.3

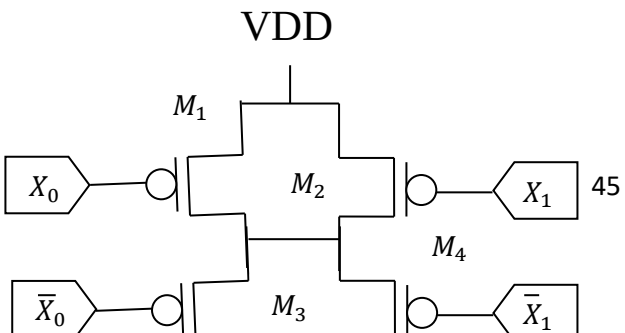
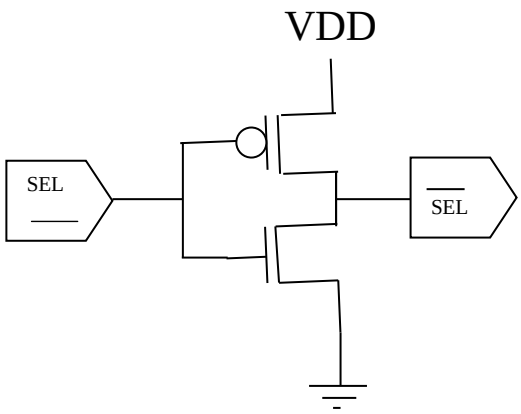
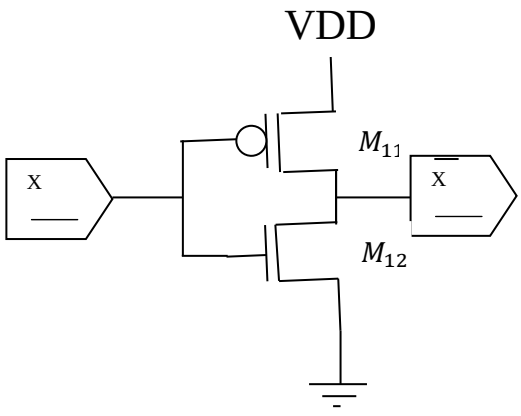
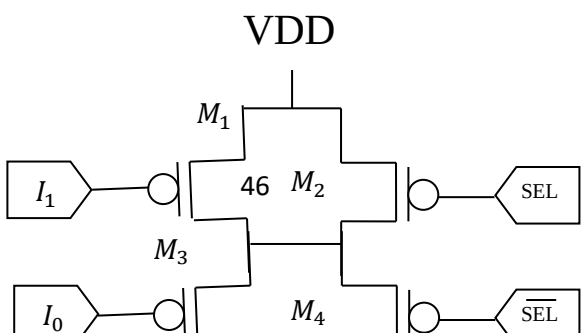


FIG.1.4 A Single bit Adder module (fig1.2, fig1.3, fig1.4).







Adder)

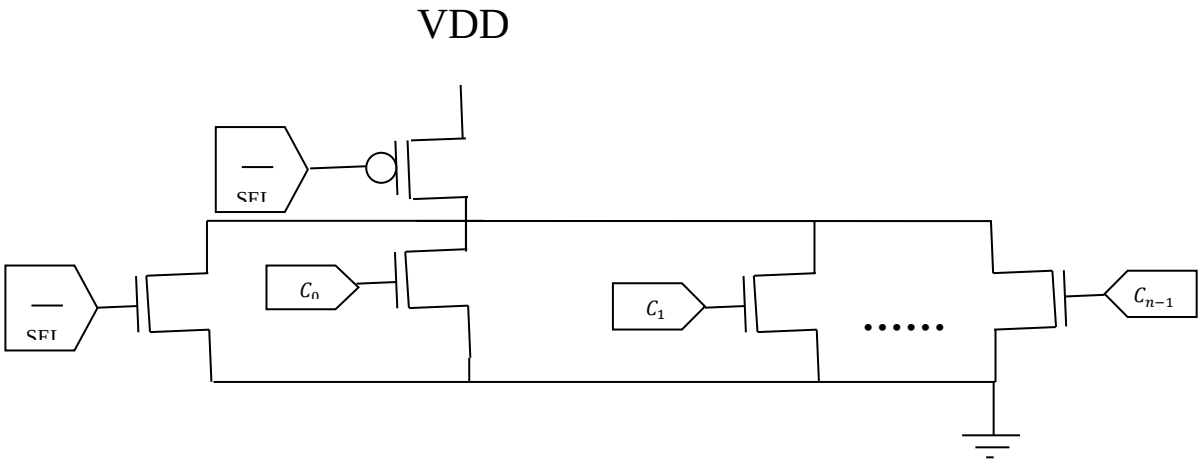


Fig. 1.6(The Termination signal generation circuit)

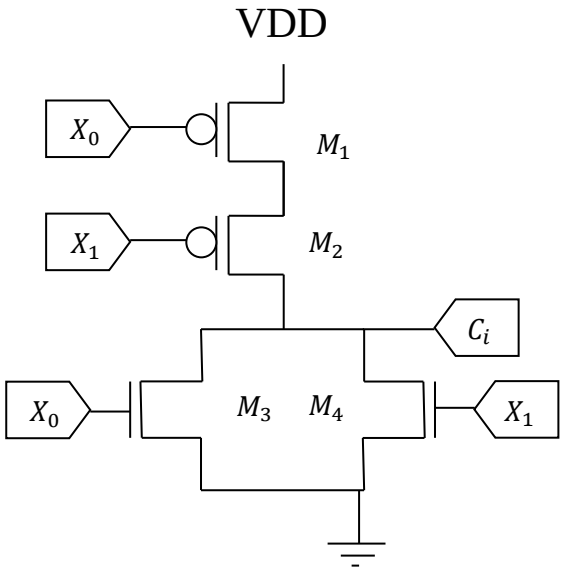


Fig.1.7 (A Signal Bit carry module)

The CMOS implementation of each module in as shown as fig [1.2-1.7].The research work here utilizes stacking power gating for reduction of leakage power, ground bounce noise as well as active power in conventional A parallel self time adder. Conventional bit full adder stages. Where ST1, ST2 is sleep transistor wait have high threshold voltage and reduce the leakage current in idle mode. The Stack Transistor (ST1 and ST2) reduce the stand by current .The wait mode is also use in Active mode & +Sleep mode to discharge the virtual ground voltage, During Sleep to active mode. This can be divided into two parts which reduce ground bounce noise. In Active mode it is waiting. The delayed of ΔT in activation of transistor NM6.in short period of mode delay ΔT isolate the ground. The drain current is control by the capacitor C2 with ST1 (Stack Sleep transistor) V Bias (FBB) voltage is apply in PWT (Transistor).It reduces the Threshold voltage for wait transistor and reduce the voltage of wait Transistor. And during sleep to wait mode, the virtual ground voltage discharges.

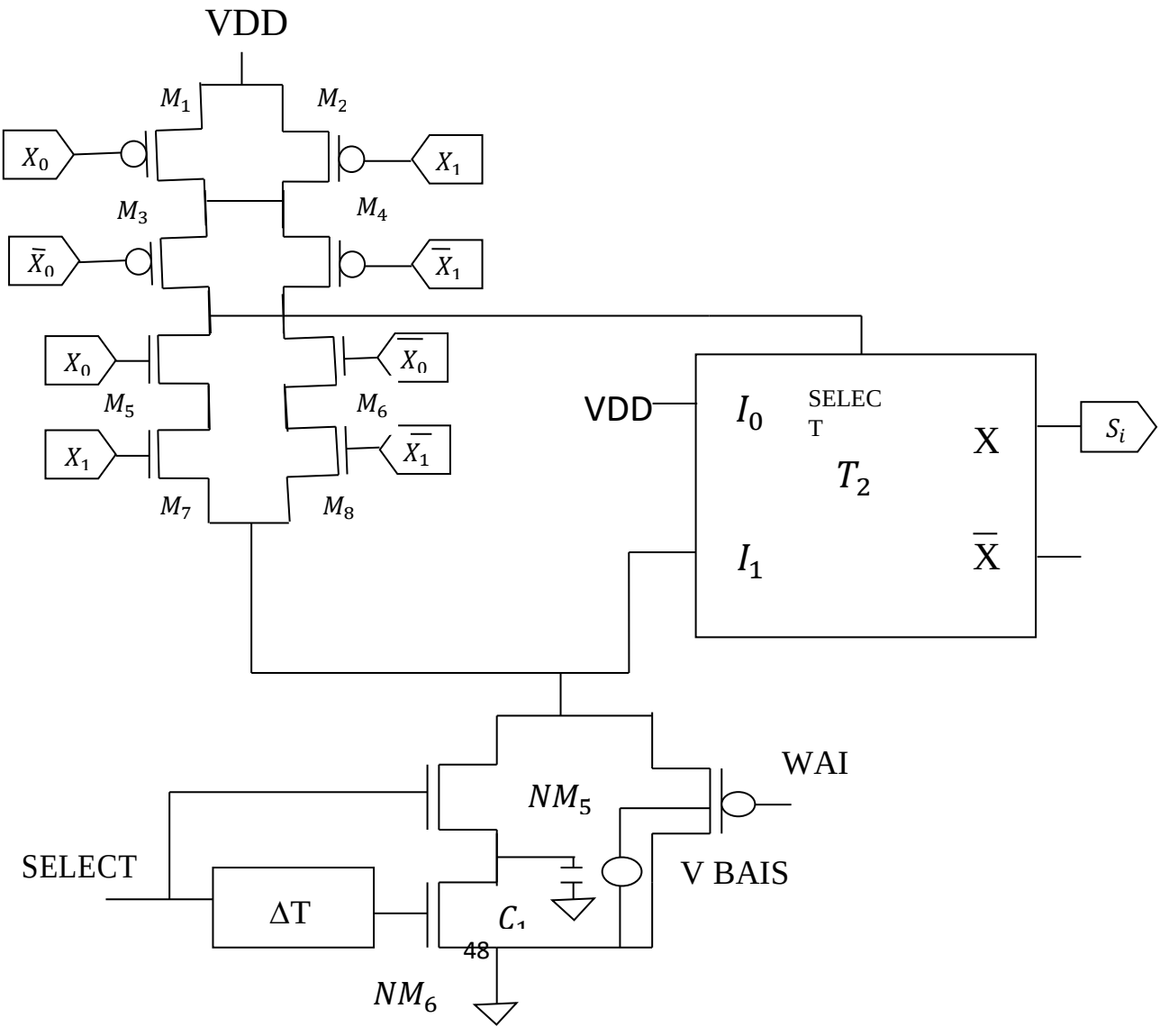


Fig.2.Modified 4 bit A Parallel self time Adder with forward body biased multimode MTCMOS Techniques.

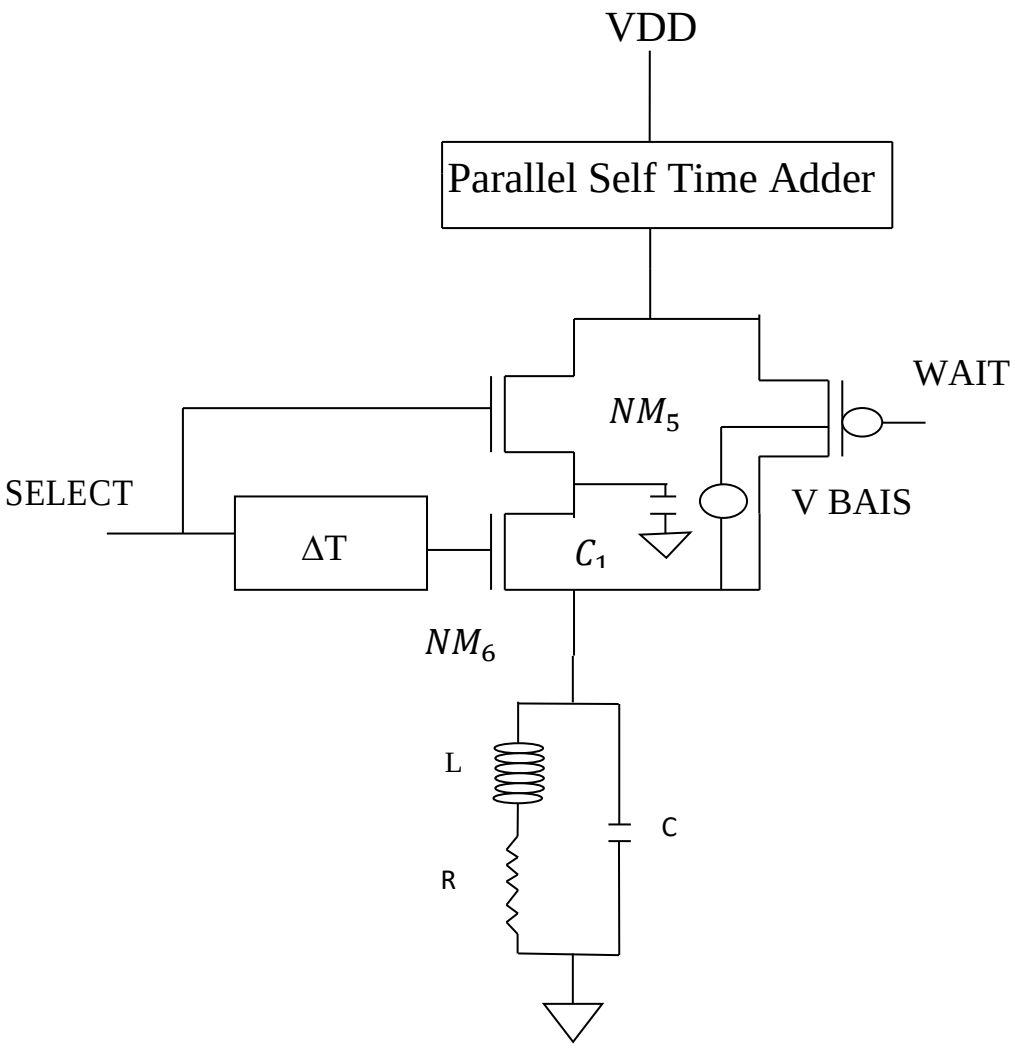
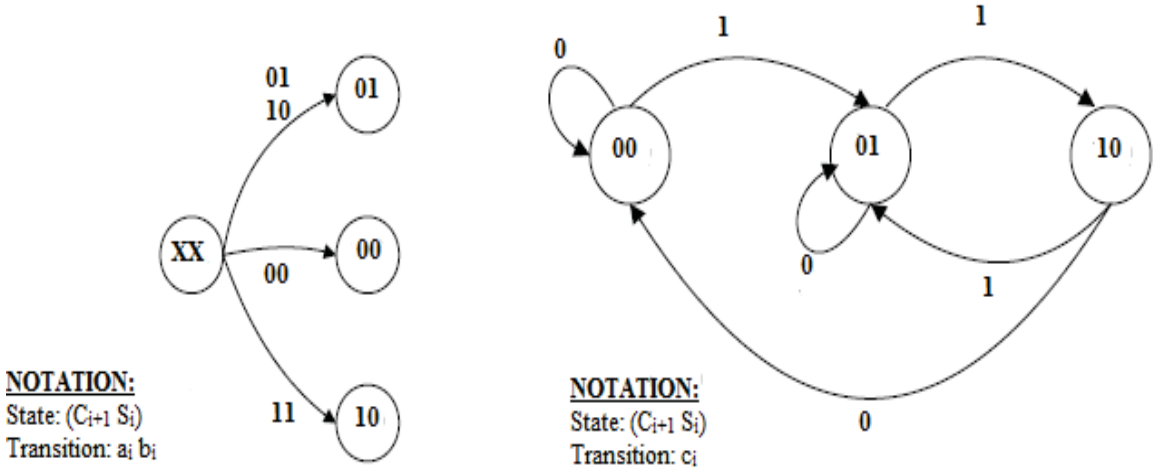


Fig.3.Modified 4 bit A Parallel self time Adder with forward body biased multimode MTCMOS Techniques and ground bounce noise.

State Diagrams:

Two state diagrams are drawn for the initial phase and the iterative phase of the PASTA architecture as in fig 4.Each state is represented by (Ci+1Si+1) pair where Ci+1, Si+1represent carryout and sum values, respectively, from the bit adder block. During the initial phase, the circuit Merely works as a combinational HA is operating in fundamental mode. It is apparent that due to the use of HAs instead of FAs, state (11) cannot appear during the iterative phase (Sel=1), the feedback path through multiplexer block is activated. The carry transitions (Ci) are allowed as many times as needed to complete the recursion. From the definition of fundamental mode circuits, the present design cannot be considered as a fundamental mode circuit as the input–outputs will go through several transitions before producing the final output. It is not a Muller circuit working outside the fundamental mode either as internally; several transitions will take place, as shown in the state diagram. This is analogous to cyclic sequential circuits where gate delays are utilized to separate individual state.



(a) Initial phase (b) Iterative Phase

Figure.4: Initial and Iterative Phase State Diagrams for PASTA

PERFORMANCE ANALYSIS AND SIMULATION RESULT

In this section we are performing simulation of our Parallel self time adder (adder with FBB Multimode MTCMOS) on cadence aether tool.

The Active power is dissipated by the circuit. When the circuit is operation state. The Active power consumption of CMOS circuit [22] is consumed by following equation.

$$P_{active} = P_{dynamic} + P_{static} \quad (1)$$

$$P_{active} = P_{switch} + P_{short} + P_{leak} \quad (2)$$

$$P = \alpha_{0\to1} \times C_1 \times F_{clock} \times V_{dd}^2 + I_{short-circuit} \times V_{dd} + I_{leakage} \times V_{dd} \quad (3)$$

Where, $\alpha_{0\,to1}$= probability, C_1=load capacitance, F_c=Clock Frequecy, Vdd=power supply, I_{short} =short circuit current, I_{leak} =leakage current As shown the table 1. figure(2) and (3) in the case of modified 4 bit a Parallel self time adder with forward body biased multimode MTCMOS active power is reduced compared to conventional A Parallel self time adder .The reduction almost 57.71 % at voltage 0.7 V and temperature 27^0 C.

TABLE I. ACTIVE POWER DISSIPATION OF A PARALLEL SELF TIME ADDER

Circuit	Cont.PASTA		Modified PASTA	
Supply and temprature	.7v	27℃	.7v	27℃
Active power(nw)	110.5	110.5	46.65	46.65

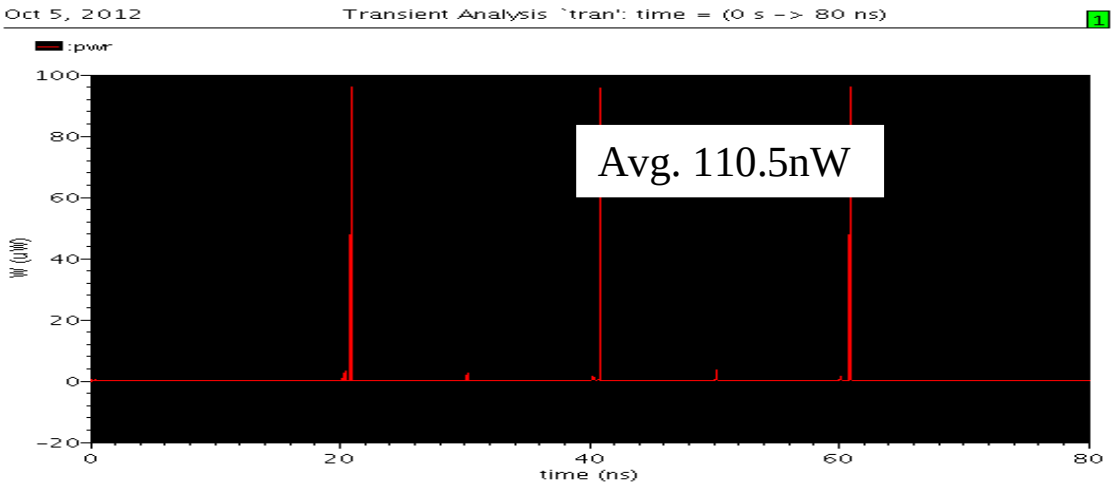


Fig.5.Active Power of conventional 4 bit PASTA

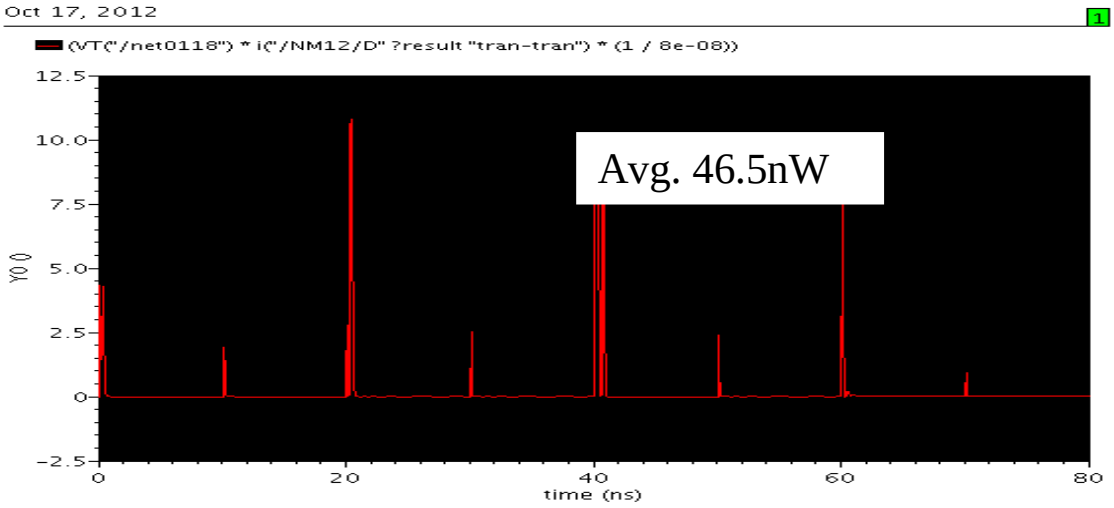


Fig.6.Active Power of Modified 4 bit PASTA

TABLE II.STAND BY LEAKAGE CURRENT AND POWER DUE TO VARIOUS VOLTAGE

Volt(v)	Leakage Current		Leakage Power	
	Cont. Pasta (nA)	Modified Pasta (PA)	Cont. Pasta (nw)	Modified Pasta (pw)
0.5	92.54	47.34	30.16	101.84
0.7	159.30	79.29	71.58	114.10
0.9	231.40	158.10	144.40	134.13
1.1	282.50	219.10	292.80	144.69
1.3	344.40	400.10	347.40	225.35

TABLE III.STAND BY LEAKAGE CURRENT LEAKAGE POWER DUE TO VARIOUS TEMPERATURES

Temp.℃	Leakage Current		Leakage Power	
	Cont. Pasta (nA)	Modified Pasta (PA)	Cont. Pasta (nw)	Modified Pasta (pw)
27	159.56	79.37	71.15	114.23
47	161.54	140.65	177.38	256.87
67	163.43	250.21	79.72	388.62
87	166.21	320.43	81.32	444.26
107	194.56	426.07	91.42	572.31

B. Standby Leakage Current:

We connect sleep transistor between the PASTA and ground of circuit. Both Transistors is off; when we measure the leakage current in forward biased multimode [11].The basic equation of stand by leakage is [22].

$$I_{leakage} = I_{sub} + I_{ox} \quad (4)$$

$$I_{sub} = K_1 W e^{-Vth/nV_0} \left[1 - e^{-\frac{V}{V_0}}\right] \quad (5)$$

Where, I_{sub} = threshold leakage current I_{ox}= Gate oxide current.

Where k1 and n is experimentally derived, W is gate width, Vθ is thermal voltage, n slope shape factor/ sub threshold swing coefficient, V_{th} is threshold voltage.

$$I_{ox} = K_2 W [\frac{V}{T_{ox}}]^2 e^{-\alpha T_{ox}/V_0} \quad (6)$$

Where K_2 and α are experimentally derived, Tox is oxide thickness.

Stand by leakage current is measured by at 0.7V and 27. The table II, III and figure (7), (8) shows the leakage current at various voltage and various temperature℃ is greatly increase reduced almost 50 % in modified PASTA with forward body biased multimode MTCMOS.

C. Leakage Power:

We measure the leakage Power, when sleep Transistor is off. The stand by leakage current is the product of the leakage current and supply voltage [22]. The basic equation of leakage Power is

$$P_{leakage} = I_{leakage} \times V_{dd} \quad (7)$$

Where V_{dd} =Power supply, $I_{leakage}$ =Leakage current, P_{leak} = Leakage power. As shown this equation this power is reduced by different parameter and it is depending on V_{dd}. So reduced the power, we reduce the V_{dd}.In this paper we want the reduce the power consumption.

The table II, III and fig.(9),(10) show that leakage power is reduced in various voltages and temperatures after applying forward body biased multimode MTCMOS. Stand by leakage power is measured at 0.7V and 27 ℃ it is greatly reduced almost up to 70 % in modified 4 bit adder with forward body biased multimode MTCMOS.

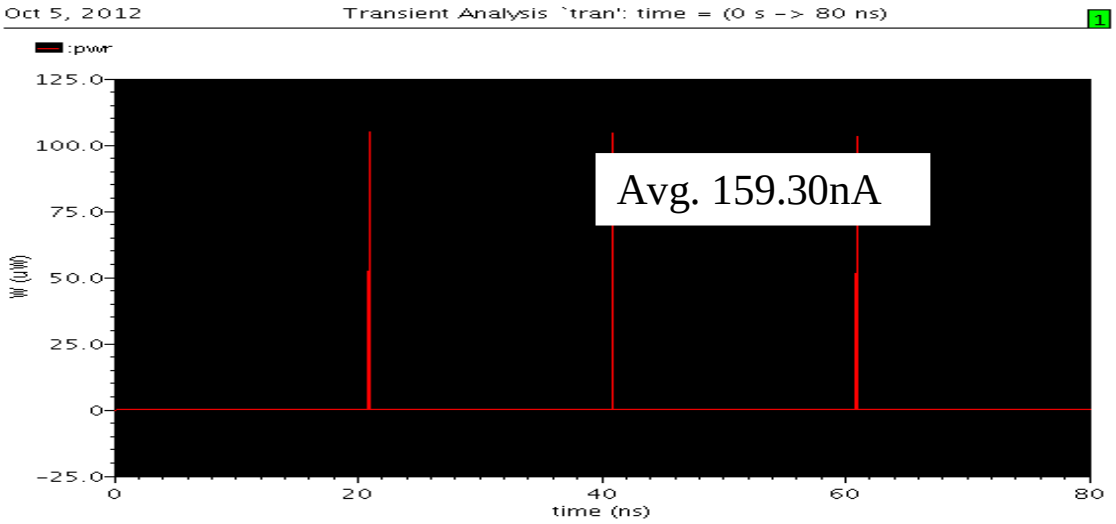


Fig.7.Leakage Current of conventional 4 bit PASTA

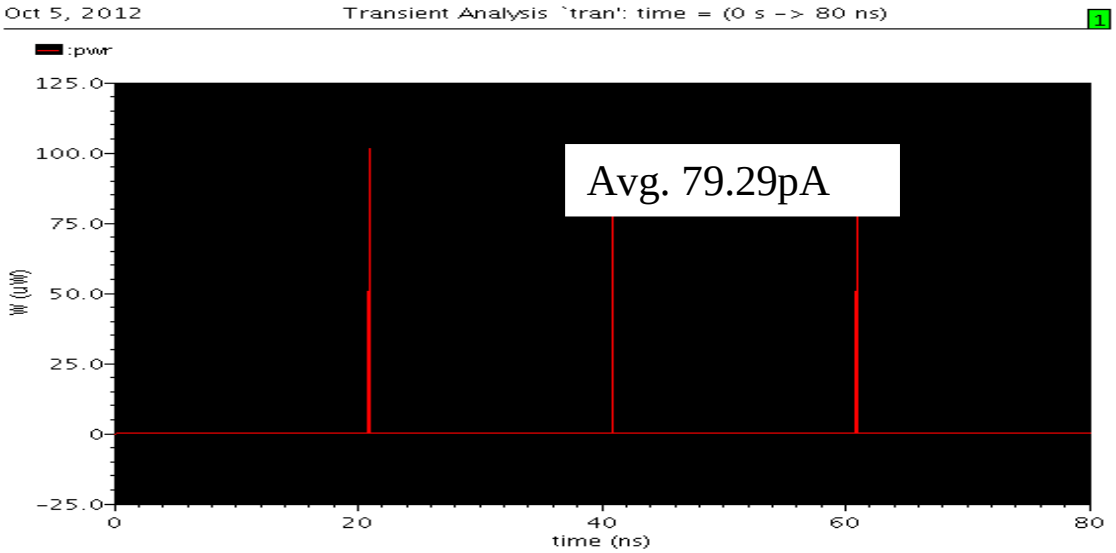


Fig.8.Leakage Current of modified 4 bit PASTA

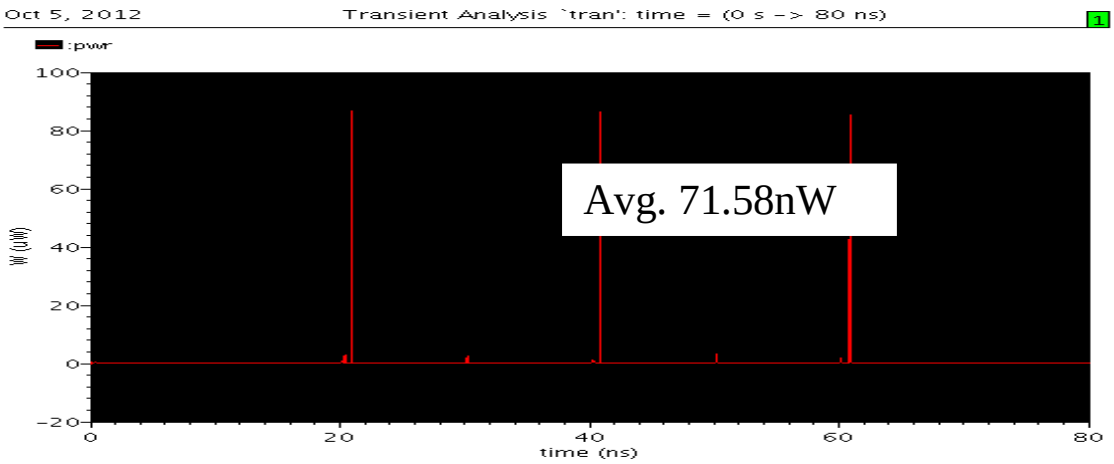


Fig.9.Leakage power wave of conventional 4 bit PASTA

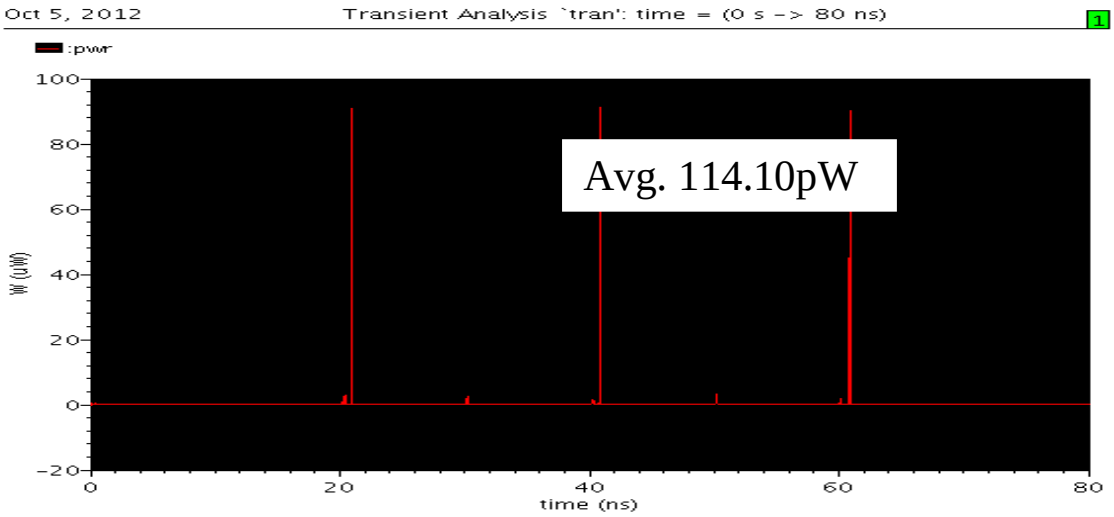


Fig.10.Leakage power wave of modified 4 bit PASTA

D. Ground Bounce Noise:

An instant current pass from sleep transistor when the circuit is Active mode. This is saturation region. And sudden current increases. The region behind is inductance of the off- chip because of self and parasitic inductance on chip power rail result voltage function in the circuit depends on input / output buffers and internal circuitry. The ground bounce noise is reduced upto 90% in this circuit various voltage and current. As shown in the table IV and fig. (11), (12), the noise depends on the voltage.

TABLE IV. GROUND BOUNCE NOISE OF 4 BITS PARALLEL SELF TIME ADDER

Voltage(v)	Ground Bounce Noise (nv)		Temp.℃	Ground Bounce Noise (nv)	
	Cont. Pasta (nA)	Modified Pasta (PA)		Cont. Pasta (nA)	Modified Pasta (PA)
0.5	67.32	19.34	27	64.62	41.85
0.7	64.65	41.75	47	67.43	34.26
0.9	97.43	65.41	67	70.34	45.31
1.1	126.92	90.23	87	75.67	54.32
1.3	158.14	116.91	107	81.41	64.93

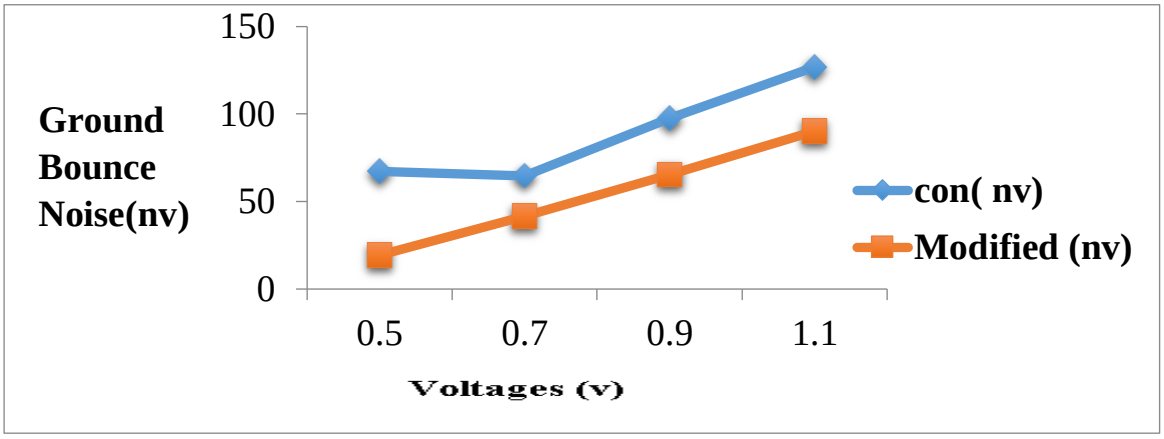


Fig.11.Ground Bounce Noise graph of PASTA at various Voltages

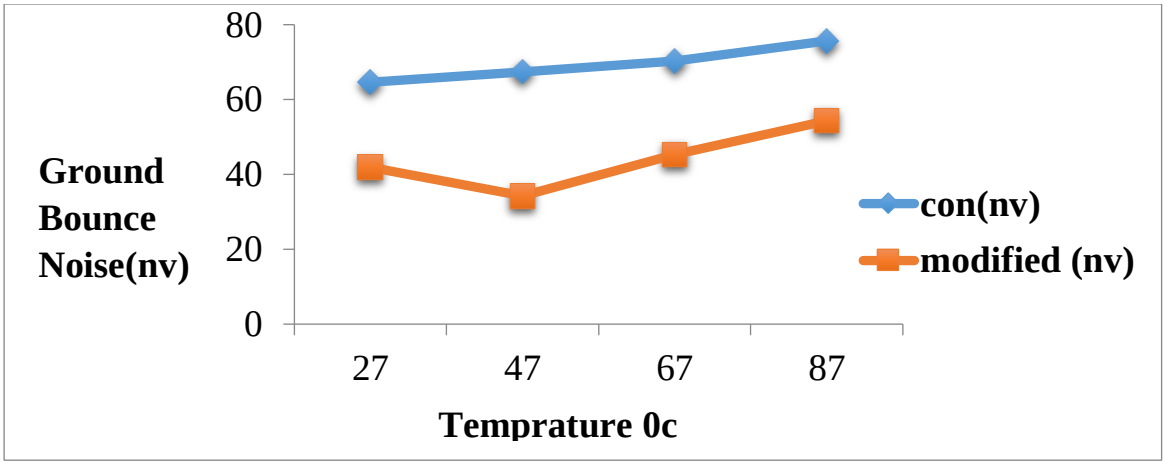


Fig.12.Ground Bounce Noise graph of PASTA at various temperature

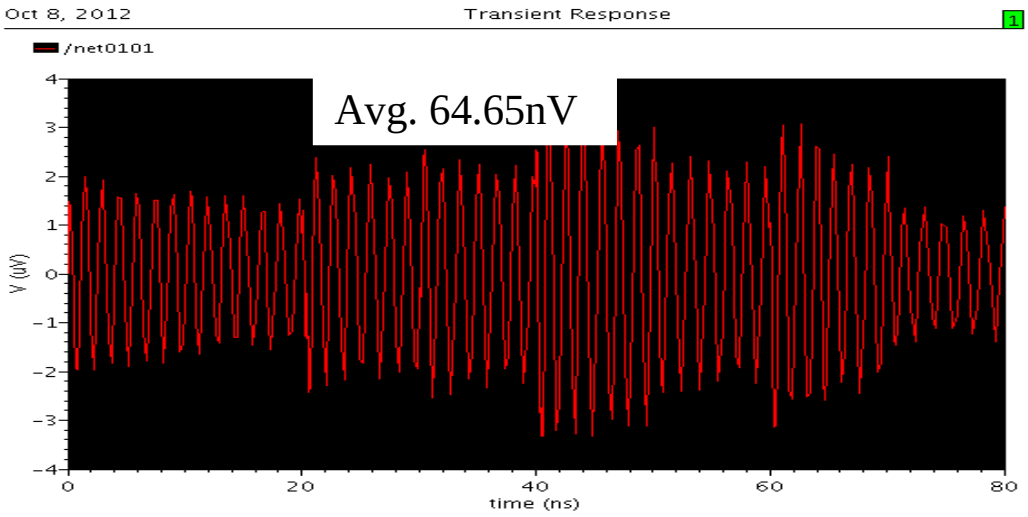


Fig.13.Ground bounce noise of cont PASTA

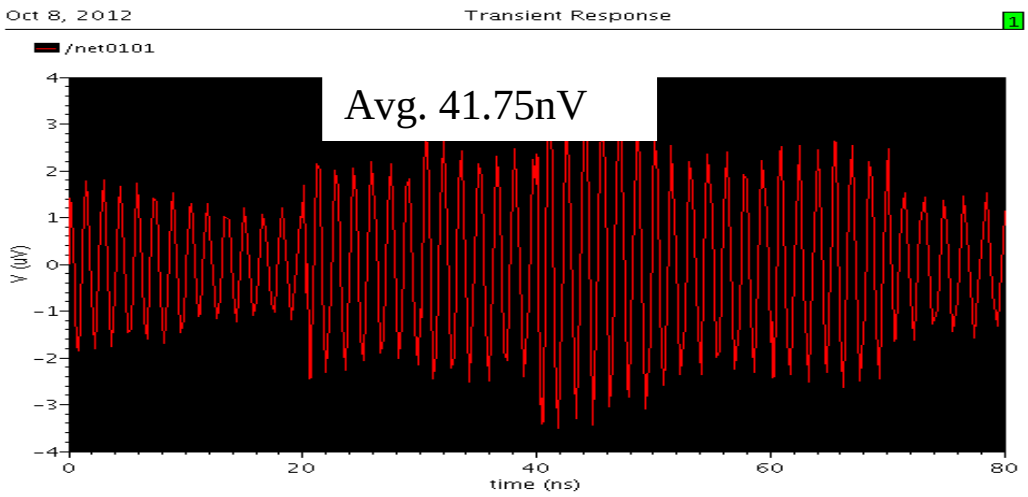


Fig.14.Ground bounce noise of modified PASTA

Conclusion:

In this paper we have used high performance forward body biased(FBB) multimode MTCMOS technique to reduced active power, leakage power, leakage current and ground bounce noise. Here we proposed a modified 4 bit Full Adder for high performance microprocessor and arithmetic logic circuit with low ground bounce noise and reduce leakage power The leakage current up to 50% and leakage power up to 70 %. The ground bounce noise is reduced to up to 40 % and active power is reduced up to 57.71 %.The proposed modified 4 bit adder is operated at various voltages and various temperatures.

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