Design and Implementation of Arithmetic and logical unit Using FinFETs

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Abstract: ALU is the core of all microprocessors. It also a combination of logic blocks to perform the logical or arithmetic operations. Now a days ALU is getting more complex and smaller in size to make the development of smaller and most powerful computer systems. This project designs An ALU using MOSFET as a conventional method. In conventional ALU consumes a large amount of power and also consist some limitations during scaling down such as short channel effects, gate dielectric leakage etc. The proposed ALU designed with a FINFET. It has powerful control on short channel effects while scale down the size of the transistor. The design simulation is carried out in H-spice simulation tools. Finally power has been studied and also compared between the ALU designed using MOSFET with proposed FINFET based design of ALU.

Keywords: FINFET, short channel effects (SCEs) ,Device simulation, ALU ,H-Spice

1. INTRODUCTION

An Arithmetic Logic Unit (ALU) performs logical or arithmetic operations. An Arithmetic logic unit is Very important part of the central unit processor (CPU) .An ALU is the also integrated packages, in this package comes the arithmetic and logic circuitry. It is getting smaller and more complex nowadays to enable the development of a more powerful but smaller computer. However, there are a few limiting factors that slows down the development of smaller and more complex chip when CMOS is used. The primary obstacles in scaling the bulk CMOS are short channel effects, sub-threshold leakage and gate-dielectric leakage. In the design of circuits like ALU fabricated with nanometer CMOS technologies, the handling of power consumption and, in particular, the tradeoff between leakage power and dynamic performance is a challenge. The strategies to tackle this issue involve all the abstraction levels of the design. From the viewpoint of the electron devices, multi-gate FETs realized in a thin silicon film offer good electrical characteristics and an attractive biasing flexibility.[1]

Fin FET has a very good control on short channel effects in the sub-micron regime thus increasing the possibility to scale down the transistor. Due to this reason, the small length transistor can have a larger intrinsic gain and a very less off-state current compared to the bulk counterpart. Drain to source capacitance is very less

which leads to reduction in power consumed. In addition, there is no “reverse body effect” in these transistor devices. It has an improved latch-up, noise, and current immunity through the substrate.[3]

2. BASIC ALU STRUCTURE

The basic design of ALU consists of a control unit made up with a multiplexer and the operation unit consist of different kind of operations like and or subtraction addition. A simple design of ALU is shown in Figure 1.1

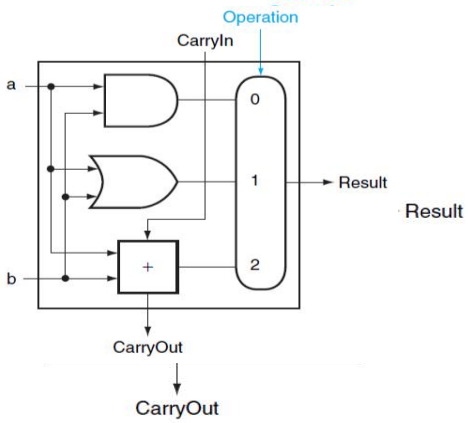


Figure 1.1: 1-bit ALU

2.1 BASIC CMOS STRUCTURE

MOSFET are generally categorized into two types, n-type MOS (NMOS) and p- type MOS (PMOS) device. The NMOS device fabrication is carried out on a substrate of p-type also called the bulk or body of the device. It consist of Highly doped two n-regions which forms the source and drain terminals .A piece of polysilicon has not heavily doped which operating as a gate ,and a silicon dioxide (SiO_2) with thin layer which seperates the gate and p-type substrate. The basic diagram for MOSFET as shown in Figure 1.2.Consider a PMOS structure, where the device fabrication is carried on a n-type substrate and consist of not lightly doped two p-regions. The thin SiO_2 seperates the gate terminal from the n-type substrate .In MOSFET, the conducting channel is formed between the source and drain region. The complementary manner operation of PMOS and NMOS is called as a CMOS (complementary MOSFET).

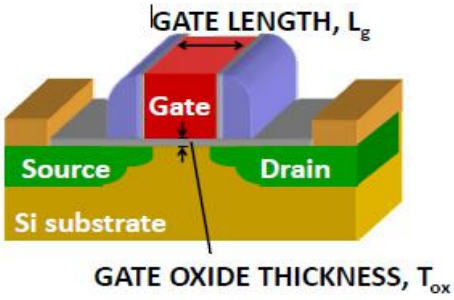


Figure1.2: Diagram for MOSFET

3 BASICS OF FINFETs

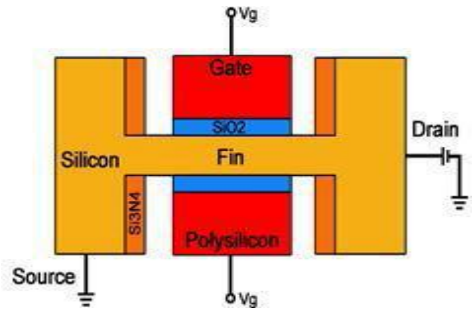


Figure 1.3: Structure of FINFET

The structure of FINFET as shown in Figure 1.3. FINFET transistor technology is a new concept to the VLSI designers. The first FINFET was fabricated a two-gate on a SOI structure as called a single gate transistor. FINFET term was explaining the non planar, two-gate transistor which fabricated on a SOI se most relevant substrate that depends on the basic single gate transistor model. The most relevant characteristics of FINFET that the channel formed between source and drain due to the electron flow conduction is covered with a thin silicon "fin", which implement the body of the transistor. Effective length of the channel is equivalent to the thickness of the silicon fin. In order to raise the channel in FINFET, it used a "fin".

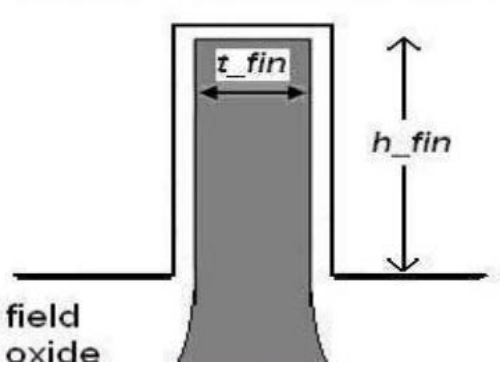


Figure1.4: Effective channel length and width of FINFET

Figure 1.4 shows the effective channel length and width of the FINFET. The gate has a very good control over the carriers presented in the device, if the channel shape is very thin. This shape gives the limitation to flow of current at low level when the device is switched ON. If the back gate of the FINFET is biased with a voltage like non-zero, it gives a result of reduction in the leakage current, with an increment of delay[10].

4. DESIGN IMPLEMENTATION

These days the exponential increment of portable devices required a less power consumption, lesser area and increased speed of operation. As the package density of a chip will increases when the transistors number increases in single silicon chip. The leakage power is increasing where the technology related with CMOS process is reduced. The main aim of device scaling is that reduces the space which is used, increasing the speed of operation and applies a best control to the channel with the configuration of gate. The important factor in any circuit design is the decreased consumption of power. The suitable way of reducing the power in a circuit is to decrease the supply voltage. The leakage current in a gate because of thin t_{ox} and the sub threshold leakage current because of small value of v_{th} are the different design factors related with the increasing leakage current. Here the sub threshold leakage current is nothing but the current flows from the drain region to the source region, when the transistors are in off condition. The sub threshold leakage current will also occurs where the transistor threshold voltage is greater than the gate to source region voltage. In a circuit, the gate leakage current is nothing but the flow of current to the substrate from the gate through the insulator layer of oxide[15]. The following sections discuss about the ALU design with existing CMOS structure and proposed FINFET structure.

4.1ARITHMETIC AND LOGIC UNIT

ALU is the important building block of any digital system design, which gives the arithmetic and logical operation functions. Various bit width of ALU is recently required for in the field of very large scale integrated circuit design. The enhanced computer and digital processing applications causes to the more demand for low power and high speed operations. In order to get the better performance in signal processing and image processing, the throughput of arithmetic operations should be high. Multiplication, division, addition, subtraction are the major arithmetic operations.

5. CONVENTIONAL MOSFET ARITHMETIC AND LOGIC UNIT

In conventional method, the 1-bit arithmetic and logic unit is designed using MOSFET with 180nm technology. Here the ALU performs one arithmetic and seven logical operations including addition, AND, NAND, OR, NOR, EXOR, EXNOR and INVERTER. The circuit also consists of an 8:1 multiplexer.

The block diagram for a 1-bit ALU as shown in Figure2. The diagram of ALU was designed in the transistor level with MOSFET.

The 1-bit ALU diagram generally designed with the help of different circuit modules such as full adder, multiplexer etc.

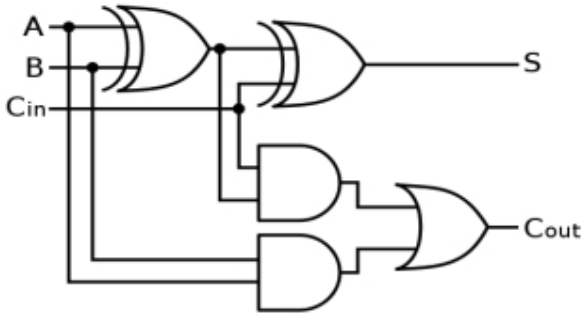


Figure 2.1: 1-bit ALU

5.1 FULL ADDER

The full adder circuit is a combinational circuit. This circuit provides the sum output of the three input bits. Generally a full adder circuit includes three input bits and two output bits. The inputs bits are nothing but, it included a one bit for A, one bit for B and one bit for the carry input. The circuits give the two output likes sum and carry out. So the sum gives the results after adding the bits A, B, carry input. Consider a device or circuit consists of more bit of ALU, there it will use carry out as the input of next ALU.

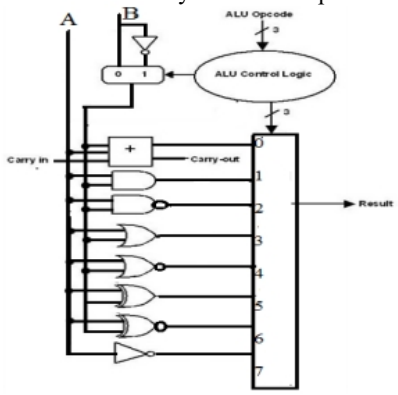
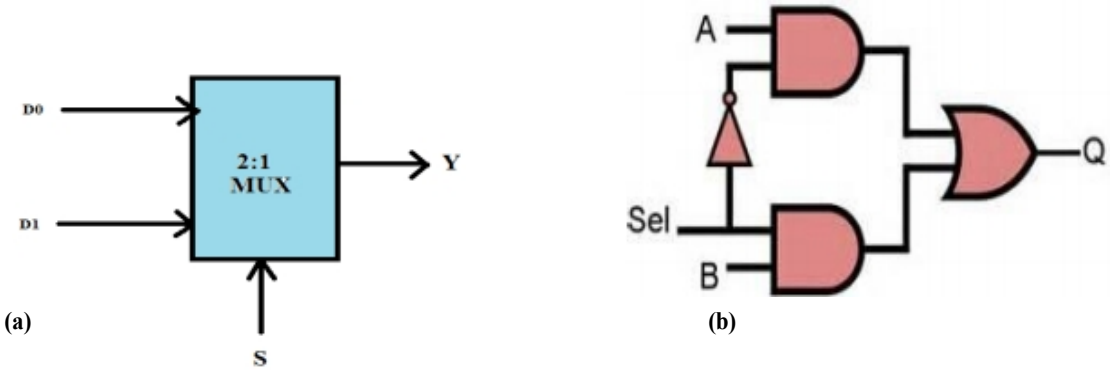


Figure2.2: Full adder

5.2 MULTIPLEXER

Here the ALU control logic is an 8:1 multiplexer. The multiplexer was implemented in the transistor level using MOSFET. It will select the required input for the arithmetic logic unit. Here the 8:1 multiplexer was designed by using 2:1 multiplexer module. When the all select lines s2, s1, s0 bits are equal to zero, then the ALU will perform the arithmetic operation. If the s0 bit is equal to one and other select lines are zero, the ALU will perform the AND operation. According to the Table 2.1 the ALU perform the other operation also. In CMOS technology, mainly three factors are causes to the power dissipation, such as static power, dynamic power and short circuit power. The static power will occurs when the circuit is inactive. It is also a "product of the power supply voltage and static or dc current. The static current flow occurs due to the parasitic diodes". The dynamic power is the major factor involved in the power consumption. Dynamic power occurs due to the "charging and discharging of the gate capacitance during switching". So the total capacitance of a gate circuit is the effective part in power consumption. In order to minimize the transistor capacitance, the designer should concentrate on the transistor sizing.



(c)

Figure 2.3: (a) 2:1Multiplexer,(b) Circuit diagram of 2:1 multiplexer(c)8:1 multiplexer

Table 2:1 operation of ALU

6. PROPOSED FINFET ARITHMETIC AND LOGICAL UNIT

Due to the scaling limitations in CMOS technology introduced a device with new concept like multi-gate device. Small scaling technology became too difficult in the MOS device. So the designers went to use a FINFET the MOS device. So the designers went to use a FINFET MOSFET based ALU is replaced with FINFET. The ALU having architecture blocks same as in existing method like arithmetic and logical unit. But the transistor level circuits are different. The FINFET have different modes of operation. In that one of the mode of operation is followed by the ALU designs.

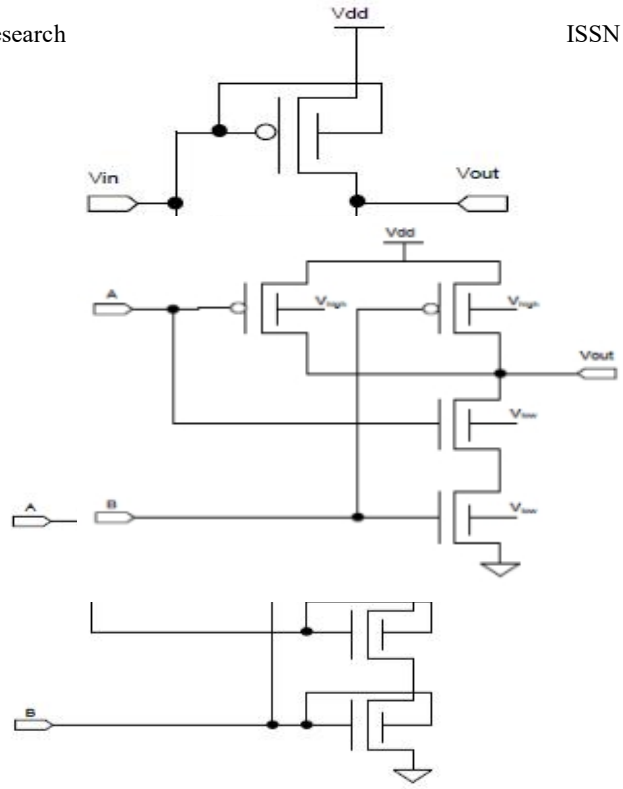
DIFFERENT MODES OF OPERATION:

1. Short Gate(SG) mode.
2. Low Power (LP) mode.
3. Independent –Gate (IG) mode.
4. Hybrid IG/LP –mode

SHORT GATE (SG) MODE:

In shot gate mode of operation both gate of the FINFET are shorted to get the improved performance like better control to the channel length. The Figure 2.5(a) shows the short gate mode inverter design and Figure 2.5(b) shows the short gate mode NAND gate.

S2	S1	S0	Function
0	0	0	Arithmetic
0	0	1	AND
0	1	0	NAND
0	1	1	OR
1	0	0	NOR
1	0	1	EXOR
1	1	0	EXNOR
1	1	1	INVERTER



(b)

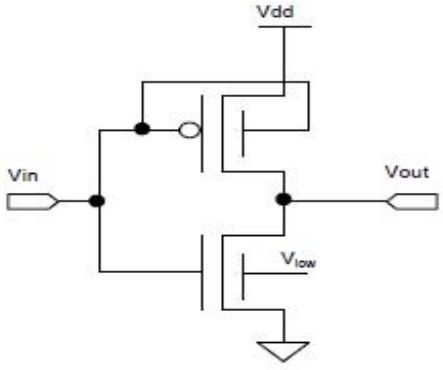
Figure 2.5: Short gate mode circuit (a) Inverter, (b) NAND

(1) LOW POWER (LP) MODE:

In this mode a low voltage is applied to back gate of the n-type and a high voltage is applied to back gate of the p-type FINFET transistor. There is a reduction of leakage power dissipation with an increased delay due to the variation of threshold voltage. Figure 2.6 (a) shows the low power mode inverter where the back gate of the p- type transistor is biased with a high voltage like 1V and the back gate of the n-type transistor is biased with a -0.2V. Figure 2.7 (b) shows the Low Power mode NAND gate.

(2) INDEPENDENT –GATE (IG) MODE:

The two gates of the device is driven by the independent signals. So the number of transistor in the circuit may be reduced. Figure 2.7 (a) shows the independent mode inverter. Figure 2.7 (b) shows the independent gate mode NAND gate. Here only one p-type transistor is used and it is connected with two input signal, one is connected to the front gate and another is connected to the back gate. The n-type transistors are kept in the short gate mode.



(a)

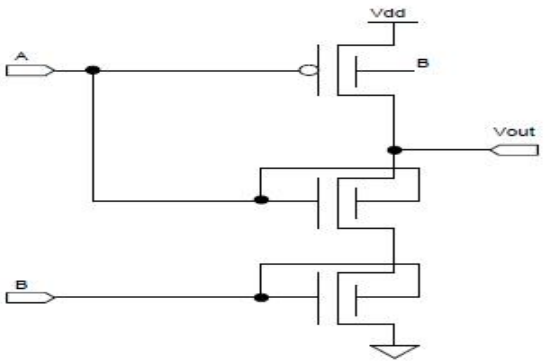


Figure 2.7: Independent Gate circuit (a) inverter, (b) NAND

3.HYBRID IG/LP MODE:

The operation mode is done with Independent mode and Low power mode.

RESULT

A. DELAY AND POWER CALCULATION

The delay is calculated as the time difference between 50% of rise in input to 50% of rise in output. The fall delay
is calculated by the time difference between the 50% of fall in input to 50% fall in the output. The delay of sub blocks
is given in Table I, below which show the results for delay in both FinFET and MOSFET.

Table I: Delay of ALU Design operations

Operation	FinFET	MOSFET
Addition	39.21ns	51.9ns
Subtraction	59.30ns	89.60ns
AND	0.19ns	3.80ns
OR	0.99ns	40.1ns

In the Figure 2.8, it shows the delay graph between MOSFET and FinFET it shows the variations in delay for each sub block in FinFET is better than MOSFET.

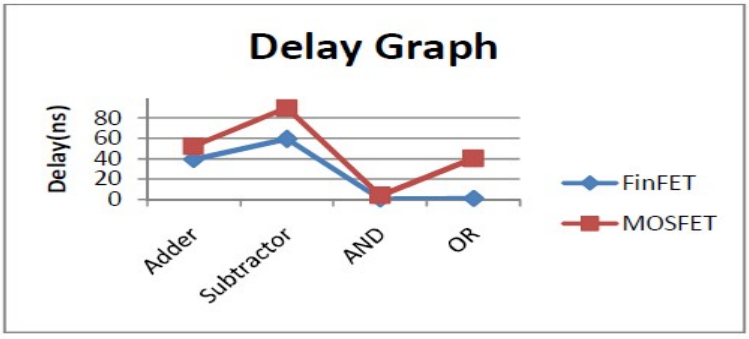


Figure 2.8 Delay graph of MOSFET and FinFET

Average power calculated for FinFET is less than MOSFET. Table II, below show the average power of the sub blocks
using MOSFET and FinFET.

Table II: Power of ALU Design operations

Operations	FinFET	MOSFET
Addition	0.041nw	24.45uw
Subtraction	0.097nw	19.5uw
AND	0.098pw	3.65uw
OR	0.10pw	1.25uw

In the Figure 2.9, it shows that the average power variations between MOSFET and FinFET for each sub-block of ALU and also shows that average power in FinFET is less than MOSFET.

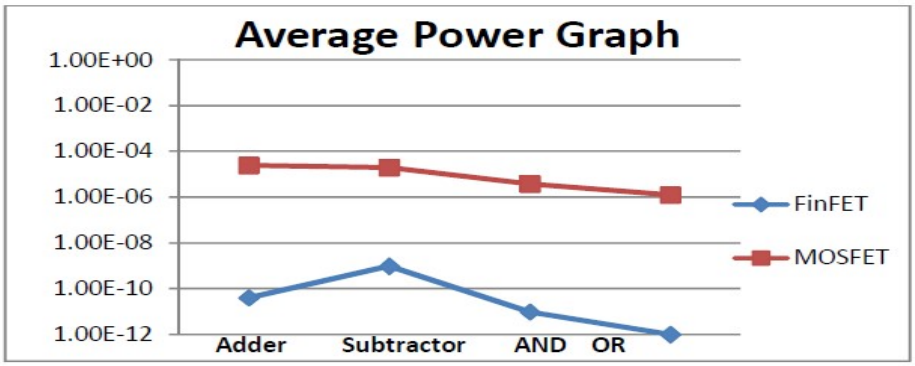


Figure 2.9 :Average Power analysis of MOSFET FinFET

From both the architectures the average power and delay has been calculated below in table III, From this Table it is observed that delay and average power consumed by FinFET is far less than the delay and power consumed by MOSFET which results that the FinFET have faster speed less power dissipation than the MOSFET.

Table III: Comparison between Power and delay of FinFET and MOSFET

	Delay	Power
finFET	4.49ns	24uw
MOSFET	67.2ns	0.318mw

In the Figure 3., it Shows the power and delay variations in FinFET and MOSFET. In delay calculation it shows thedelay obtained in MOSFET is far more than the delay obtained in FinFET. Also in power calculation it shows the average power consumption by FinFET is less than MOSFET

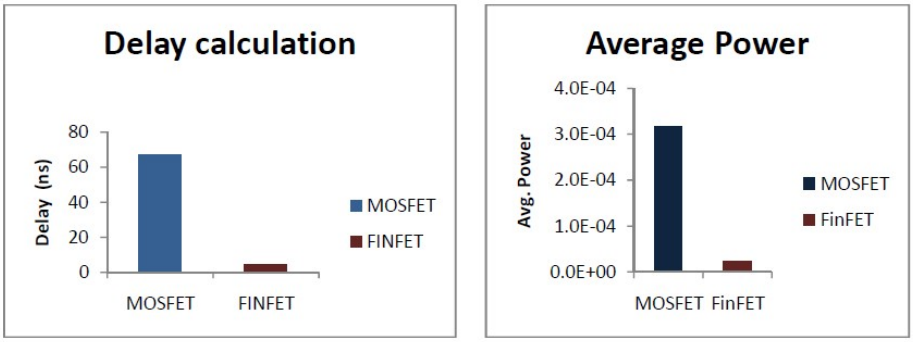


Figure 3: Delay and Power in MOSFET and FinFET.

CONCLUSION

This project designed and implemented an ALU by using FINFET as well as MOSFET. The ALU include the arithmetic and logical operations. It is shown that results obtained for proposed FINFET ALU consumes less power compared with the conventional MOSFET ALU. The ALU designed in 180nm technology and FINFET ALU designed in the SG mode. During scaling process the FINFET design is better to use in the VLSI technology field. The simulation will be carried out using H-SPICE tools.

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