Modelling and design optimization of Latch Circuits (CMOS NAND Gate Based) by using the Parametric Timing Analysis Technique

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Abstract- The contemporary computing era demands ultra fast, high performance memory circuits to perform on line operations in synchronization with high turbo-speed microprocessors. Since nano scale technology necessitates the need of accurate latch models, realization of ideal latch models becomes crucial. But latch devices face some parametric and time-domain constraints, which thwart it to perform better. For the correct data storage, voltage level sensitive latches are widely used with high performance circuits where timing analysis is more significant and challenging job. The Parametric Timing Analysis (PTA) Technique enables us to optimize any prototype model at designing phase itself. Application of PTA Technique also takes into account the external timing variations and their impact on Rise-Fall time, *Setup-Hold time, Toggling conditions,* Propagation delay and metastability etc. The CMOS NAND gate based latch circuits are implemented and simulated by using the Cadence Specter design tool in 45nm technology. Simulation result shows that ignoring accurate latch modeling may lead to large digital/analog errors like leakage power may overshoot up to a value larger than total dissipation power and output results would be erroneous or latch circuit may get damaged after specified operational limitations.

Keywords: *Parametric Timing Analysis (PTA) Technique,* Setup time, Hold time, *Rise time, fall time Propagation delay, Toggling, Leakage power, Total dissipation power.*

I. INTRODUCTION

Today in nano-era age, process variations are imposing the biggest challenge to technology scaling regime by being a major performance limiter. Parametric Timing Analysis (PTA) technique has been proposed to perform full-chip analysis of timing under process variations and has been the subject of intense research recently. To attain more accuracy, PTA technique is done by considering the clock distribution network. By these approaches one can predict both the data signal's statistical distribution at the end of each combinational logic chain and the parametrical distribution at each terminal of the network [1]. The major challenging task is designing more accurate Flip-flop and latches, which are the most commonly, used in sequential elements whose purpose is synchronizing data signals. These elements will add some delay to timing and thus decrease the system performance, which leads us to concentrate on latch models accurately [2]. The approaches presented in this literature, the latch delay model is deterministic; being parametric quantities the impact of the input data signal and clock pulse has been analyzed on the variation of output data as leakage current, leakage power, total power, rise time, fall time, setup time, hold time and propagation delay. Based on this new latch delay model, one can combine the timing analysis of data signal to the clock distribution network to do parametric timing analysis in an accurate way [2-8]. The main contributions of this paper include: a) a CMOS NAND gate based latch timing model considering both logic and clock signal variations by varying the clock frequency and (b) integrating the proposed latch model into the parametric timing analysis.

The rest of this paper is organized as follows: [9-13]

a.) Normal timing diagram and structure of designing latch are reviewed.
b.) New point of view for the latch working model based on Parametric Timing Analysis.
c.) It is a latch model taking into account ultra-speed variations for optimum utilization.
d.) Result and the conclusion is drawn in the last section.

II. LATCH PRELIMINARIES

The latchh is actually a feedback based digital switch, which can be put to two states (SET or RESET) everlastingly till supply is available. Latch indicates bi-stable states of material, property, conditions and electronic flow eg. Magnetic-diamagnetic, open – closed door, crest-turf on DVD track, etc. A latch is a three-terminal element, having two inputs VIN, clock (clk /C) and output (Q). [11-14].

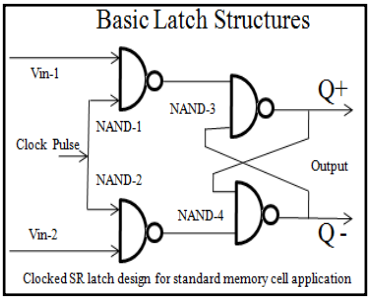


Figure: 1

a.) Truth Table of SR latch

A latch is a three-terminal element, having two inputs, data (S & R) and clock (clk /C) and two outputs (Q+ & Q-). A. State transform into a latch storage part If the two NAND gates in the storage part of the latch are the

same and driving strength of the PMOS and NMOS in each NAND are also identical, the potential of the storage part can be drawn as Figure 1. All latches were following four special state points: [15-16]

Point A (V1=0, V2=0), Stable with highest logic Storage state
Point B (V1=0, V2=Vdd), Stable on lowest logic
Point C (V1=Vdd, V2=0), Stable on logic high Set state
Point D (V1=Vdd, V2=Vdd), Metastable Toggling

Truth Table S R Latch (NAND Gate)						
S.No.	**CL K**	**S**	**R**	**Q+**	**Q-**	**Function**
01	0	0	0	Latch	Latch	No Change
02	0	0	1	Latch	Latch	No Change
03	0	1	0	Latch	Latch	No Change
04	0	1	1	Latch	Latch	No Change
05	1	0	0	Q+	Q-	Storage State
06	1	0	1	1	0	Reset
07	1	1	0	0	1	Set
08	1	1	1	1-?	1-?	Intermediate state

b.) Structure of NAND GATE BASED SR latch

One of the most widely used latch structures is shown in Figure 1. In the semi-custom data path application, where the noise of the input signal can be well controlled, this latch structure is preferable for its compactness and speed. Subject latch is designed with the CMOS NAND gate application, the latch structure (Figure 2 (a)) becomes robust and is widely used in standard cell applications. In this paper, we focus on modelling the latch structure in Figure-1 but our modelling is generic enough to be applied to the latch structure in Figure 2 (a) too [18-20].

c.) Traditional timing model of latch

The data must be stable to setup before the falling edge of the clock is called the setup time and hold after the falling edge of the clock called hold time. This feedback system has two stable states (point A & B) and one metastable state (point C) as shown in Figure 2 (b). [19,20]

tDQ = r [ln AV –ln a(0)]..... (1)

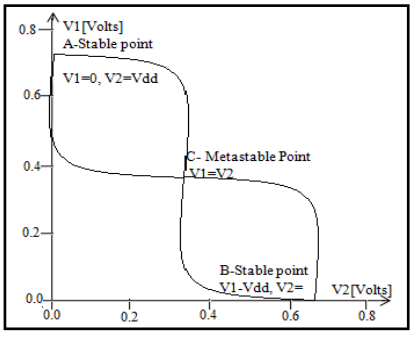


Figure: 2(a)

Where tDQ is the delay from input D to output Q, and a(O) is a small signal offset from the original metastable point. X V is some predefined constant voltage point to predict D-to-Q (tDQ) delay.[21,22] . As shown in Figure 2 (c),

(i) The storage part of a latch;

(ii) Butterfly curves of the static transfer characteristics;

(iii) An analogy of a ball on a hill with one metastable state at the top of the hill and two stable states in the foothills.

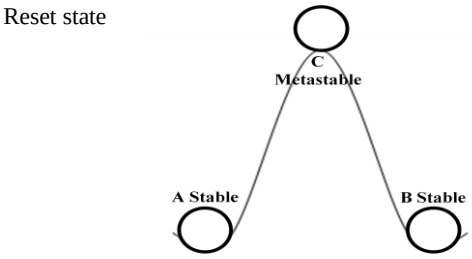


Figure: 2(b)

III. NAND Gate: CMOS Transistor level circuit and Layout diagram

The latch in Figure-1 can be decomposed into 2 parts: the input part containing a pair of NAND gates with clocking system, Storage part is cross-coupled feed-back in two NAND gates latch.

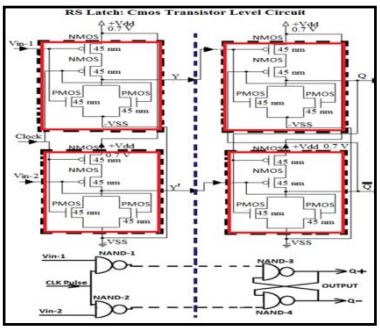


Figure: 3(a)

Layout: SR Latch (CMOS NAND Gate Based)

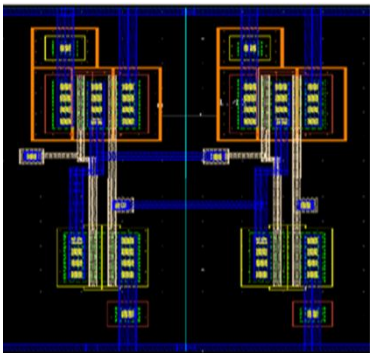


Figure: 3(b)

The above layout view has been designed using 45 nm scale technology and implemented various test like DRC (design rule check,), ASSURA LVS and design extracted with RCX.

I. Timing diagram of latch

The timing diagram of the latch is shown in Figure Both setup and hold times of a latch are measured relative

to the trailing edge of the clock. The data signal must be a constant in the timing window between the setup and hold time. [1,2] This ensures that the data is sampled and latched correctly. In addition to setup and hold Times, two more delay quantities tCQ and tDQ, need to be defined. This is because of the following two scenarios:

i) Data is stable, but the latch is quite closed due to the clock being low, and

ii) Data stabilizing while the latch is open.

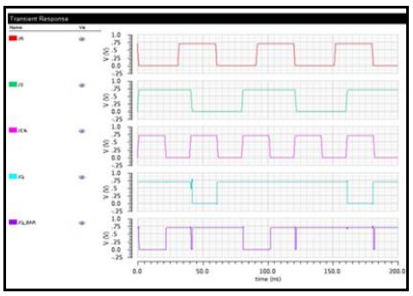


Figure: 4.

In critical path analysis, we assume that the signals arrive close to the setup time while latch is open; tDQ is the delay to be analyzed. In this paper, we focus on optimal utilization of proposed latch model at increasing order of clock. Frequency is selected on the basis of Nyquist rate (Sampling theorem) calculated from input data pulse (Vin1 or Vin2).

II. Parametric Analysis of Latch circuit

a.) Total Average Current

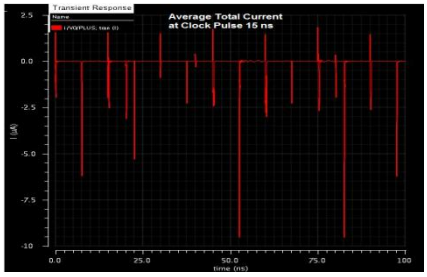


Figure: 5(a).

This parameter approves the phycal design feesibility and possibility of proposed circuoit. Total average current also determines the nature of all the input and output parameters and design indurance with varying nature of input parameters.

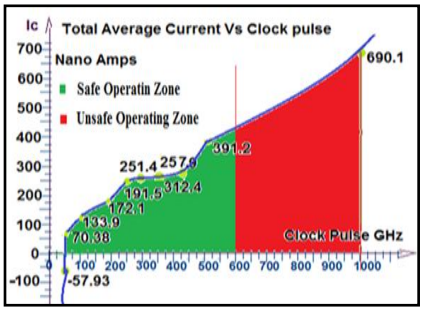


Figure : 5(b).

III. SIMMULATION AND RESULTS

During simulation phase, it has been observed that compatibility and stability of total average current of proposed latch circuit is feasible for clock frequency up to 600 GHz (Green region of the curve) and beyond this point results becomes erroneous (Red region of the curve).

a.) Average leakage Current

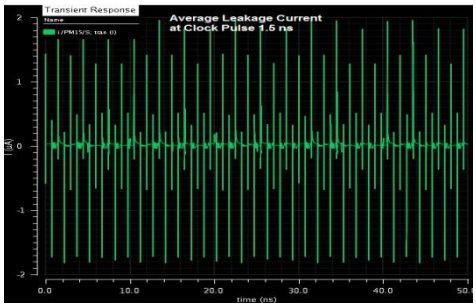


Figure : 5(c).

This parameter plays a very important role and circuit design has to be oriented towards reducing the leakage current as it drops the power while circuit is in active or idle state.

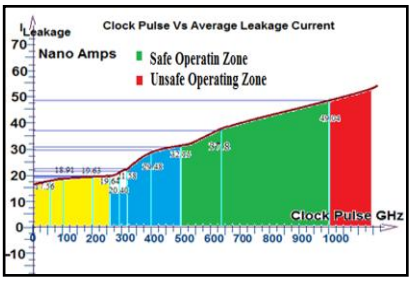


Figure : 5(d).

It has been observed that the value of leakage current increases in the circuit as per the increase gradient in operating frequency band. As its quantum and stability is very much concerned with the objective of this research work which is cleared from the above coloured regions and frequency bands. Yellow colour-less leakage current, blue colour – little value of leakage current, Green colour-good performance over the ambient temperature region..Red colour –device burning may take place .

a.) Average Leakage Power

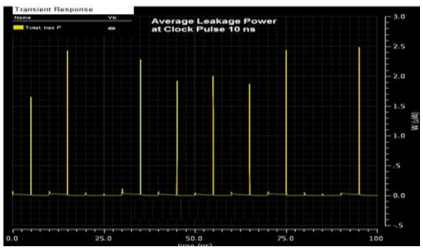


Figure : 5(e).

This parameter is again a very crucial part of the objective of this paper. PTA analysis evaluates total leakage power and impacts on the circuit designs , technology used and evaluates the reliability and layout co-ordinations between operating parameters.

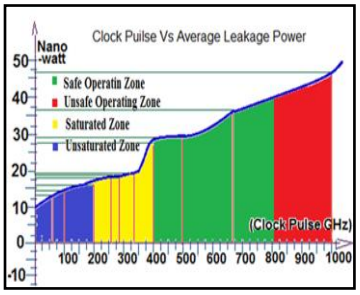


Figure : 5(f).

It has been observed that leakage power increases in the circuit as per increase in operating frequency band. But its quantum and stability is very much concerned with the objective of this research work which is cleared from the above coloured regions and frequency bands.

a.) Total Average Power

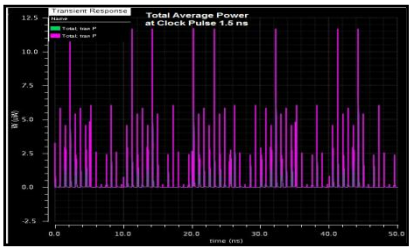


Figure : 5(g).

This parameter should be least and its value should remain stable over the complete operating frequency range it plays a very vital role in durability of the designed device.

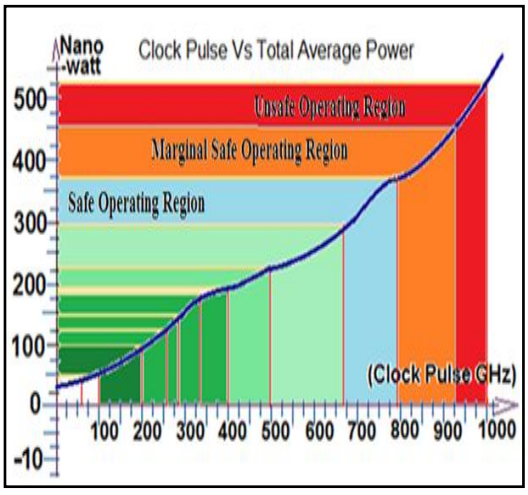
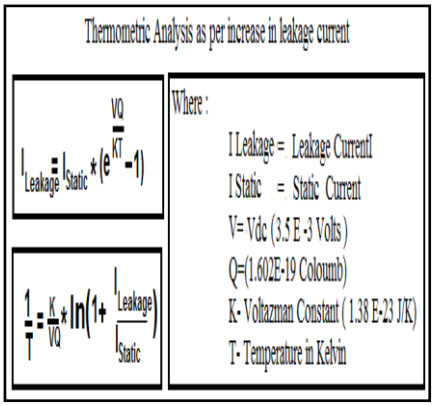


Figure : 5(h).

Power consumption and heating effects are co-related parameters which is clear from the above frequency-power curve. For operating frequency up to 650 GHz total average power is less and not causing any heating effect (Greenish region of the graph) and from 650 GHz to 780 GHz (Blue region) is uniform region at ambient temperature and above it (Red region) is unsafe in point of heat dissipation.

d.) Operating Temperature Zone: -The leakage current (Ilkg) between the layers of EGS (for the diode/transistor/CMOS) is described by the following equation:



Device operating temperature as per its Leakage current

S.No.	ClockFreqency GHz		Device Temp ^{O}K ^{O}C	Probable defects/damages	Observations
01	350	234.98	- 38.02	Best	External cooling not required
02	400	251.76	- 21.24	Better Performance	External cooling not required
03	450	271.13	- 01.87	Good performance	External cooling not required
04	500	293.72	+20.72	Parasitic Latch-up, heat.	Cooling without heat sink .
05	550	320.42	+47.42	Parasitic Latch-up, avalanche break down ,	External cooling ,heat sink , single exhaust fan required.
06	600	352.47	+79.47	Parasitic Latch-up, ESD, avalanche break down, device Burning,	External cooling with exhaust fan, heat sink and AC cooling environment required.

Parametric Timing Analysis and Simulation Results								
Test Sample	Input Parameter In nano-sec	Total Current	Total Power	Leakage Current	Leakage Power	Setup Time	Hold Time	Prop. Delay
S-01	Vin-1 =40 Vin-2 =30 Clk Pulse= 15	-57.93 n-Amp	42.43 n-Watt	17.56 n-Amp	13.34 n-Watt	230 p-Sec	67 p-Sec	917 p-Sec
S-02	Vin-1 =30 Vin-2 =20 Clk Pulse= 10	70.38 n-Amp	52.09 n-Watt	18.91 n-Amp	14.54 n-Watt	230.4 p-Sec	110.9 p-Sec	928.2 p-Sec
S-03	Vin-1 =20 Vin-2 =10 Clk Pulse= 05	133.99 n-Amp	99.66 n-Watt	19.64 n-Amp	15.91 n-Watt	230.5 p-Sec	84 p-Sec	938.5 p-Sec
S-04	Vin-1 =15 Vin-2 =7.5 Clk Pulse= 3.75	172.18 n-Amp	126.99 n-Watt	19.63 n-Amp	16.59 n-Watt	230.7 p-Sec	85.9 p-Sec	948.8 p-Sec
S-05	Vin-1 =12 Vin-2 =07 Clk Pulse= 3.5	191.50 n-Amp	148.3 n-Watt	20.40 n-Amp	16.52 n-Watt	230.69 p-Sec	91 p-Sec	950 p-Sec
S-06	Vin-1 =13 Vin-2 =06 Clk Pulse= 03	251.4 n-Amp	187.1 n-Watt	21.58 n-Amp	18.71 n-Watt	230.8 p-Sec	110.2 p-Sec	959.1 p-Sec
S-07	Vin-1 =12 Vin-2 =05 Clk Pulse= 2.5	257.9 n-Amp	196.66 n-Watt	29.48 n-Amp	27.38 n-Watt	230.9 p-Sec	111.5 p-Sec	968 p-Sec
S-08	Vin-1 =11 Vin-2 =04 Clk Pulse= 02	312.4 n-Amp	226.6 n-Watt	32.15 n-Amp	28.79 n-Watt	231 p-Sec	112 p-Sec	987.9 p-Sec
S-09	Vin-1 =10 Vin-2 =03 Clk Pulse= 1.5	391.2 n-Amp	293.6n - Watt	37.8 n-Amp	36.98 n-Watt	231.3 p-Sec	112.6 p-Sec	999.5 p-Sec
S-10	Vin-1 =03 Vin-2 =02 Clk Pulse= 01	690.0 n-Amp	520.7 n-Watt	49.04 n-Amp	40.7 n-Watt	231.5 p-Sec	116 p-Sec	1100 p-Sec

During optimisation phase the device under test (DUT) is operated ruggedly at varying operating parameters and its operating temperature has been calculated from leakage current by using above mentioned formula and tabulated below for concluding the thermal operating range.

IV. CONCLUSION

Based on a parametric perspective on latch timing an accurate latch delay model can be developed which can stand with the impact of external variations of delay and slew from input data and clock pulse. The proposed latch delay model is verified by simulations over a wide range of external variations and applied to the parametric timing analysis. Compared with existing PTA works for latch based circuits, our proposed model would prove a milestone for finalizing optimal utilization parameters with greater accuracy. Power consumption is a function of load capacitance, frequency of operation, supply voltage, technology used and operating temperature zone. A reduction of any one of these is beneficial subjected to proper analysis and optimization of parameters. A reduction in power consumption provides several benefits. Less heat is generated, which reduces problems associated with high temperature, such as the need for cooling, heat sinks. This provides the consumer with a product that costs less. Furthermore, the reliability of the system is increased due to lower-temperature stress gradients on the device. An additional benefit of the reduced power consumption is the extended life of the battery in battery operated devices. Our experimental results show that ignoring latch modeling may lead to large errors (e.g., 50% loss of power at PDF peak).

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