Analysis of Highly Stable 16-bit SRAM Array Body using Biasing Technique

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Abstract—**As Static Random Access Memory (SRAM) is used in high speed applications such as cache memory and occupies about 90% of silicon area. Various research works have been done to trim down its power consumption. There are two ways of reducing overall power consumption in CMOS SRAM these are either by decreasing the dynamic power or decreasing standby power. Subthreshold leakage, dynamic power consumption and delay are also major issues for circuits design, especially for SRAM design. Subthreshold leakage and dynamic power consumption can be decreased while Bias voltage varies accordingly. In this paper Body biasing technique is used which decrease the leakage current by 14.19% compared to the standard cells. Through using this technique, lowering supply voltage is possible. This SRAM array is working over 0.7V supply voltage offering a Delay improvement of 98% for the read cycle, and 81% for the write cycle. Read SNM is also improved by this technique. Write Margin is not affected due to using body biasing technique.**

Keywords-Body Biasing, Delay, leakage current, Dynamic power, Efficiency

I. INTRODUCTION

Technology scaling has made the current day IC's faster, denser. But faster the circuits are, more is the power consumption and hence reduces the battery life of many of the portable devices. Reduction in power consumption can be achieved by many techniques: Logic Optimization, Pipelining and parallelism, voltage scaling etc. Power reduction techniques are proposed to improve the battery life of applications such as laptop computers, personal digital assistants (PDAs), and portable communication devices. For wireless sensor network applications, due to lower frequency rate, the supply voltage may be reduced below the threshold voltage. This operation is referred as sub-threshold design that uses the sub-threshold current as drive current to evaluate the inputs[1,2]. Lowering the supply voltage reduces the subthreshold current, exponentially. Due to the effect of Vth variation on sub-threshold current, working in this region causes more sensitivity to process variations. The effect of process variation, is more important in circuits such as memories and flip-flops, that causing data loss on storage nodes in FFs or memories. Due to minimum size transistors in SRAM memories, the sensitivity to inter-die as well as intra-die process variations is significant. Failure in SRAM such as Read and Write are caused by process variations in ultra low supply voltage applications [3]. For reliable Sub-threshold applications, different SRAM topologies have been proposed. A Body Biasing technique is proposed in [3], they are adopted to reduce the leakage current on the basis that the subthreshold leakage current is exponentially dependent on the Vth.

A. *High stable 7T SRAm cell:*

The data retention of the SRAM cell in hold state and the read state are important constraints in advanced CMOS processes. The SRAM cell becomes less stable at low VDD, increasing leakage currents, and increasing variability [4]. The stability is usually defined by the static noise margin (SNM) as the maximum value of the DC noise voltage that can be tolerated by the SRAM cell without altering the stored bits [4]. The read static-noise-margin (SNM) deteriorates with decrease in supply voltage (VDD) [5] and increases with the transistor mismatch. This mismatch occurs due to variations in physical quantities of identically designed devices i.e., their threshold voltages, body factor and current factor. Though SNM decreases at low VDD, the overall SRAM delay increases. Moreover the read operation at low VDD leads to storage data destruction in SRAM [6].

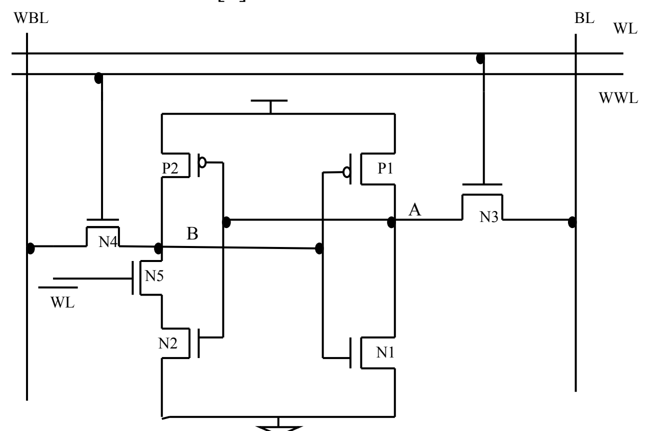

Fig.1 schematic of 7T SRAM cell

The main operations of the SRAM cells are the write, read and hold. The SNM is an important performance factor of hold and read operations [7], specifically in read operation when the wordline is '1' and the bitlines are precharged to '1'. In conventional cell the internal node of SRAM which stores '0'

will be pulled up through the access transistor across the access transistor and the drive transistor. This increase in voltage severely degrades the SNM during read operation. In order to overcome the static noise margin at low VDD 7T SRAM cell [4] is implemented in Fig. 1. It has one additional transistor compared with 6T cell but operates more efficiently than 6T cell at IOW-VDD. The 7th transistor which is nMOS transistor is between the node and the driver transistor. The voltage dividing effect takes place at the inverter which stores '0', will be pulled up. In order to stop this transition the 7th transistor at the other node is turned off so that the node which stores '1' will not be pulled down by the driver transistor as it acts a switch between the node and the driver transistor. In the data retention period, the SRAM data will not be accessed. In this period the wordline signal /WL is '1' and the nMOS transistor N5 is ON. In the read operation, the logical threshold voltage of the CMOS inverter driving node B increases when the data protection transistor N5 is turned OFF [6].

II. 16-BIT ARRAY USING 7T SRAM CELLS

A typical SRAM block consists of cell arrays, address decoders, column multiplexers, sense amplifiers, input/output (I/O), and a control unit. In our paper we use only single sense amplifier which saves tremendous power consumption. Write data can be choose from selected cell through Mux that would sensed by sense amplifier and produces read data. In the following, the functionality and design of each component is briefly discussed.

1) *SRAM Cell*: Fig. 1 shows a 7T SRAM cell. In an SRAM cell, the pull-down nMOS transistors and the pass-transistors reside in the read path. The pull-up pMOS transistors and the Pass-transistors, on the other hand, are in the write path. Traditionally, all cells used in an SRAM block are identical (i.e., corresponding transistors have the same width, threshold voltage, and oxide thickness) which results in identical leakage characteristic for all cells. However, as we will show in this paper, by using non identical cells, which have the same layout footprint, one can achieve more power efficient designs.

2) *Cell Array*: The size of the cell array depends on both Performance and density requirements. A 16-bit SRAM comprising of 4 x 4 arrays of memory cells is shown in Fig. 2. Generally speaking, as technology shrinks, cell arrays are moving from tall to wide structures [8]. However, since wider arrays need more circuitry for column multiplexers and sense amplifiers, if a small area overhead is desirable (e.g., large L3 caches), the number of rows is kept high [9].

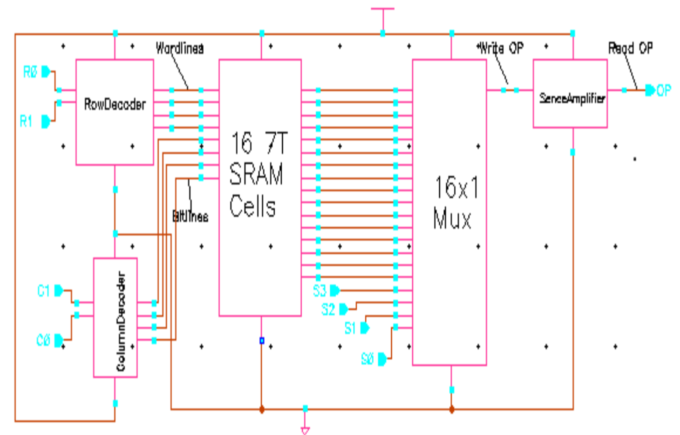

Fig.2 Block Diagram of 16 Bit SRAM Array using one Sense Amplifier

3) *Address Decoder*: Although the logical function of an address decoder is very simple, in practice designing it is complicated because the address decoder needs to interface with the core array cells and pitch matching with the core array can be difficult [10]. To overcome the pitch-matching problem and reduce the effect of wire's capacitance on the delay the decoder is designed by two input NOR gates as shown in Fig. 3a. In this design we use two bits Ao and A1 to select the row and bit A2 and A3 to select the column. Each output of row decoder controls the wordline WL of the SRAM and the each output of the column decoder control a pair of bitlines. Fig 3b presents the i/o waveform of row Decoder.

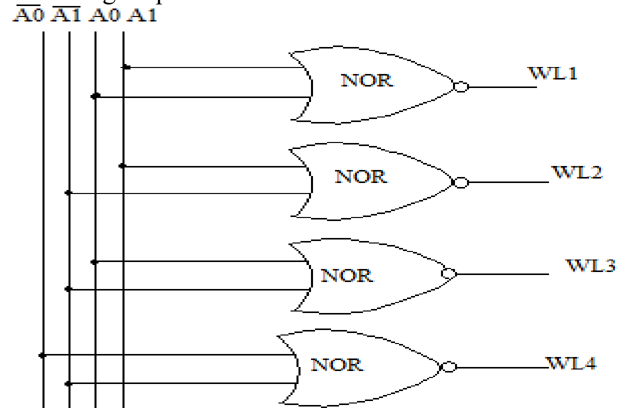

Fig.3(a) Symbol diagram for Decoder using NOR gate

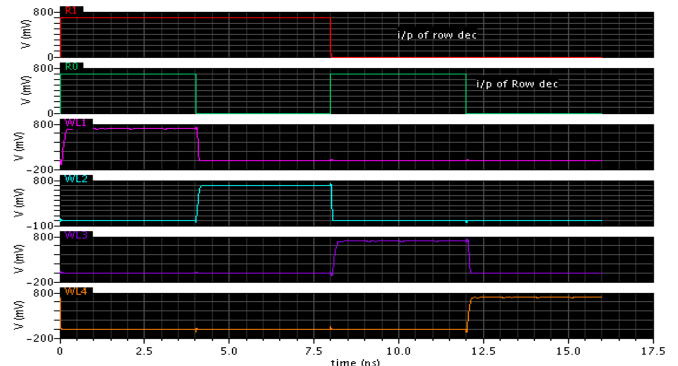

Fig.3(b) input/output waveform of Row Decoder

4) *Column Multiplexers and Sense Amplifiers*: Column multiplexing is inevitable in most SRAM designs because it reduces the number of rows in the cell array and as a result increases the speed. Here 16:1 Mux is designed using NAND gates only fig.4a, which reduces the complexity and gives better results fig.4b. Since using a read operation one of the bit or bit-line is partially discharged, a sense amplifier is used to sense this voltage difference between bit and bit-bar lines to create a digital voltage. To make the circuit more robust to noise, the sense amplifier is typically switched when the voltage difference between bit and bit-bar lines becomes 100–200 mV. In write operation the data from the write switch is written in the SRAM cell through the bitlines. In read operation both bitlines precharge and equalize to VDD and the wordline WL is turned ON. The bitline which is connected through the pass transistor to the node which is stored '0', discharges and the other bitline stays high. This charge/discharge of bitlines will then be detected by the sense amplifier through the I/0 buses.

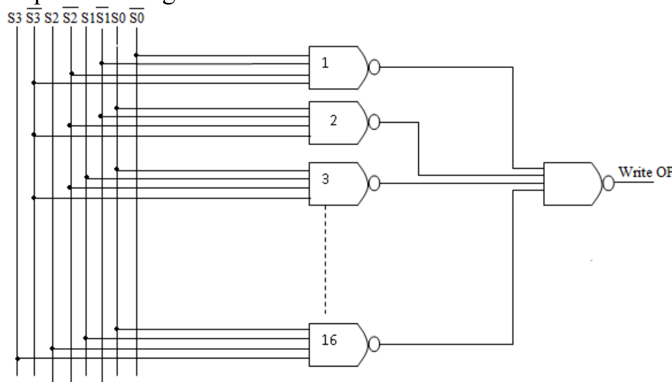

Fig.4(a) Symbol diagram of 16x1 Multiplexer using universal (NAND) gate

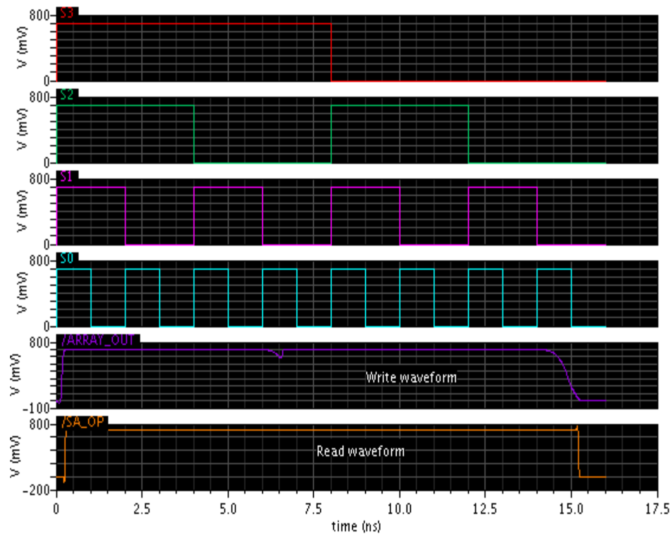

Fig.4(b) input(select lines)/output (read and write) waveforms of 16x1 Mux

5) *Control Unit*: The control unit generates internal signals of the SRAM, including the write and read enable signals, the Pre -charge signal, and the sense amplifier enabler[11].

III. DESIGN OF 16-BIT ARRAY USING PROPOSED BODY BIASING TECHNIQUE:

The body-biasing scheme is categorized as reverse body-biasing and forward body-biasing. They are adopted to reduce the leakage current on the basis that the sub threshold leakage current is exponentially dependent on the threshold voltage. As shown in Figure 5a, the reverse body-biasing scheme is applied by raising V_{NWELL} or lowering V_{PWELL} in the standby mode, to produce body effect and thus to increase the threshold voltage. Therefore, the sub threshold leakage current decreases with increasing V_{th}. In active mode, the body-biasing voltage is back to zero without affecting access time and data stability. However, extra energy and time overhead must be taken into consideration owing to the body-biasing mode transition.

The effectiveness of the reverse body-biasing scheme decreases with technology scaling, due to worsening of the body effect caused by the shorter channel length. In addition, source-substrate, drain-substrate leakage current, and band-to-band tunneling current exponentially increase at the source-substrate and drain-substrate PN junctions (because of halo doping in scaled devices)[12], proposed a dynamic Vth SRAM in which the body-biasing voltage of NMOS transistors was raised to Vth for the cells not likely to be accessed anymore. The simulation results demonstrated that a leakage current of 64 KB L1 instruction cache can be saved by 72% at 0.18 µm technology. In contrast to the reverse body-biasing scheme, the forward body-biasing scheme raises VPWELL for selected

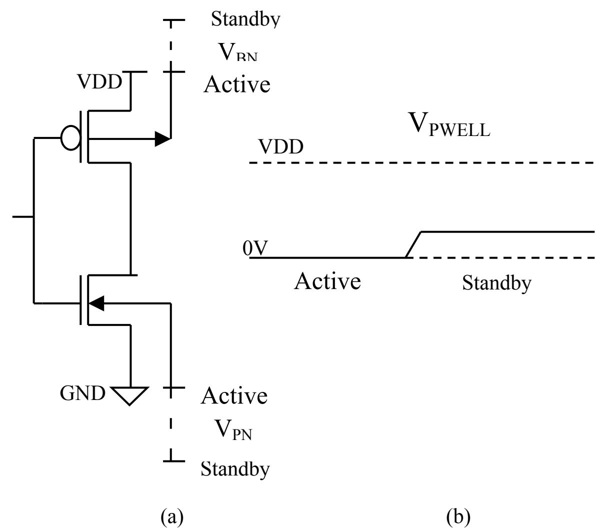

Fig.5 Body Biasing Scheme

SRAM cells, to increase the threshold voltage in the active mode so as to achieve fast operation[13]. High Vth devices built by high channel doping have been used to reduce the leakage current in the standby mode. Process complexity increases for high channel doping, where leakage mechanisms

in the nanometer regime are considered[14]. Both forward body biasing and high channel doping can improve device performance, suppressing the short channel effect and Vth roll-off. Therefore, the forward body-biasing scheme is more applicable as a technology scale. However, they have larger junction capacitance and body effect, which reduces the delay improvement, especially in stacked circuits [12]. Reverse body biasing is applied on 7T SRAM cell fig.6.

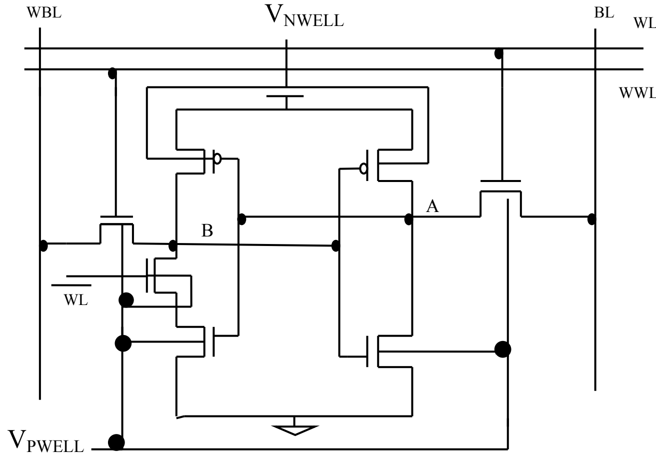

Fig.6 Schematic of 7T with Body Biasing Technique

The forward body-biasing scheme (raising VPWELL to 0.5 V) and super high Vth (350 mV) devices, to reduce cache leakage power, have been used [15]. In the case of 1.0 V supply voltage and 270 mV normal device threshold voltages, 64% leakage power reduction can be achieved for a 32 KB L1 cache. A design can use the reverse body-biasing scheme in standby mode to reduce leakage current together with the forward body-biasing scheme in active mode for high performance, which is more effective than if only one of them is used in the design. Researchers have found that forward body-biasing and high Vth devices along with the reverse body-biasing scheme provide 20 times the leakage reduction, as opposed to three times the leakage reduction for the reverse body-biasing and low Vth devices[12]

IV. PRELIMINARIES:

A. Leakage Current:

The leakage current of a deep sub micrometer CMOS transistor consists of three major components: junction tunnelling current, subthreshold current, and tunnelling gate current [16]. In this section, each of these three components is briefly described.

1)Tunneling Junction Leakage Current: The tunneling junction leakage current is an exponential function of the junction doping and reverse bias voltage across the junction. Since tunneling junction leakage current is quite small compared to other sources of leakage in state-of-the-art CMOS devices.

2) Subthreshold Leakage Current: Subthreshold leakage is the drain-source current of a transistor when the gate-source voltage is lower than the threshold voltage. The subthreshold leakage is modelled as

$$Isub = Asub \exp\left(\frac{q}{\acute{\eta} kT}\left(VGS - Vt0 - \Upsilon VSB + \eta VDS\right.\right.$$

where, Asub= μ_0 CoxW/$L_{eff}$$(kT/q)^2e^{1.8}$, μ_0 is the zero bias mobility, Cox is the gate oxide capacitance per unit area, and denote the width and effective length of the transistor, k is the Boltzmann constant, T is the absolute temperature, and q is the electrical charge of an electron. In addition, Vt0 is the zero biased threshold voltage, ϒ is the linearized body-effect coefficient,η denotes the drain-induced barrier lowering (DIBL) coefficient, and ή is the subthreshold swing coefficient of the transistor.

3) Tunnelling Gate Leakage Current: Electron tunnelling from the conduction band, which is only significant in the accumulation region, results in direct tunnelling gate leakage current in nMOS transistors. In pMOS transistors, on the other hand, hole tunnelling from the valence band results in the tunnelling gate leakage current[17].

Effect of temperature can be seen on leakage current and Delay. Fig. 7, 9a, and 9b encounter the variations in leakage current and delay respectively with different(-40°C,27°C, 110°C) temperature for both Array designs. Comparisons lead that biased array decrease leakage current as well as delay[18].

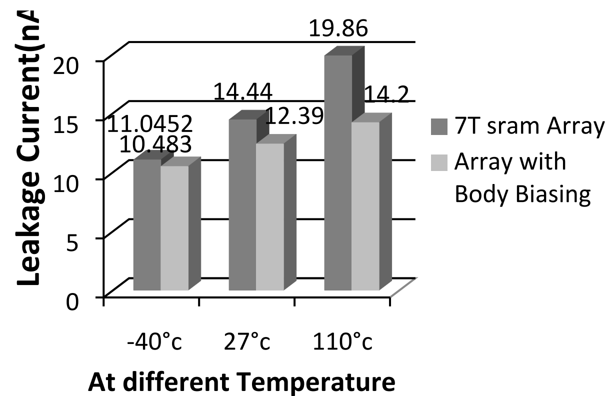

Fig.7 Comparison of leakage currents of Simple array and array with body biasing at different temperatures

As shown in Figures 8a and 8b, a higher reverse body-biasing voltage leads to a larger reduction in leakage current and it is obvious that the effectiveness of the leakage suppressing capability is better at 27°C. Raising VNWELL to 1.4 V provides the maximum leakage saving (1.27 times) at the condition of

27°C, while 1.10 times leakage power reduction is achieved for -0.4 V NMOS(VPWELL) body-biasing voltage at 27°C with raised VNWELL, whereas, reducing VPWELL increases hold-SNM and decreases read-current slightly, thus, access time increases a bit. Generally speaking, the reverse body-biasing scheme has little effect on SRAM cell stability and delay time.

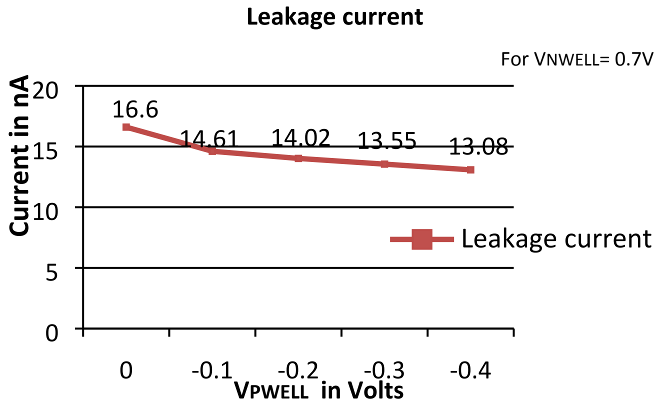

Fig.8(a) Leakage current at different VPWELL in biasing tech.

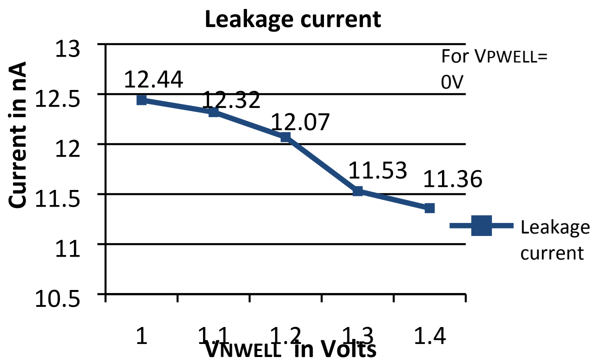

Fig.8(b) Leakage current at different VNWELL in biasing tech.

B. Delay:

In Fig. 9a and 9b shows comparison of write and read Delay is made for 16-bit SRAMs designed by only 7T and 7T with biasing cells. It is shown that the performance of using 7T with biasing SRAM cell is far better than that of using 7T cell. This is due to additional voltage supply(VPWELLand VNWELL) given to substrate of pMOS and nMOS in 7T SRAM. The write delay is measured from Data-in to the node B of the SRAM and the read delay is calculated from the wordline WWL to the sense amplifier output OP.

C. Dynamic Power:

Dynamic power consumption is due to the current that flows only when the transistors of the devices are switching from one logic state to another. This is a result of the current required to charge the internal nodes (switching current) plus the through current (current that flows from V_{DD} to GND when the p-channel transistor and n-channel transistor turn on

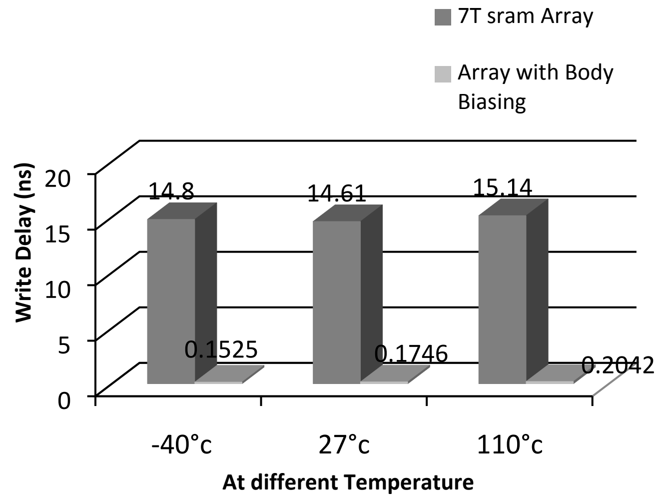

Fig.9(a) Comparison of Write Delay of both type of array

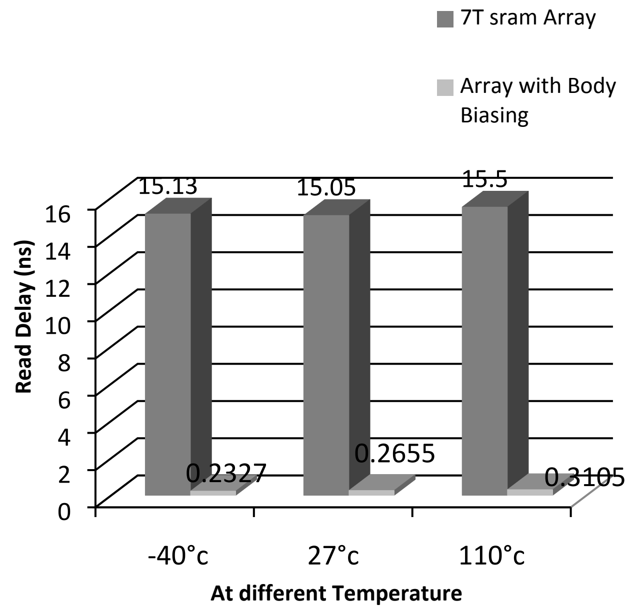

Fig.9(b) Comparison of Read Delay of both type of array

briefly at the same time during the logic transition). The formula of Dynamic Power shown in below.

$$P_{dyn}= C_L V_{DD}^2 f$$

Where V_{DD} is supply voltage ,C_L (Capacitance) is a Function Of fan-out, wire length, transistor sizes and f is Clock Freq. As seen in Fig. 10a and 10b dynamic current get reduce using body biasing technique[19].

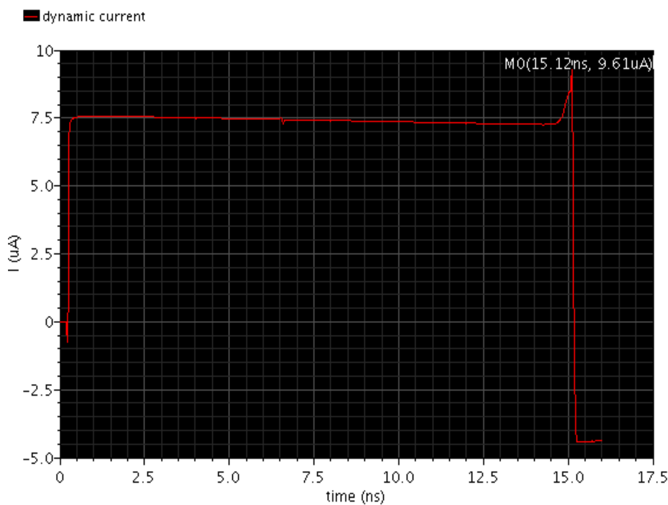

Fig.10(a) dynamic current of 7T SRAM Array

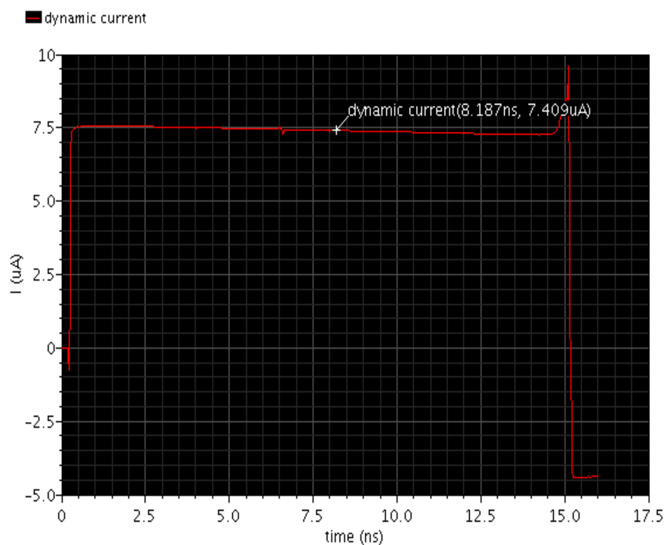

Fig.10(b) dynamic current of 7T SRAM array with body biasing

D. Operating Current/Power :

This is the maximum amount of current that SRAM consumes while it is in operation with the Vdd at the maximum, the chip select pin active, and output at high impedance. Also known as off-state leakage current and residual current. The amount of current required to keep a sensor active when it is not detecting a target, and operating power is the maximum amount of power that the SRAM consumes while it is in operation with the Vdd at maximum, the chip select pin active, and the outputs in high impedance. Operating currents for both arrays shown in fig. 11a and 11b, obvious decrement in consumption of power using body bias technique. Regarding of that operating power is 11.89 µW for former and 11.69 nW for biased array.

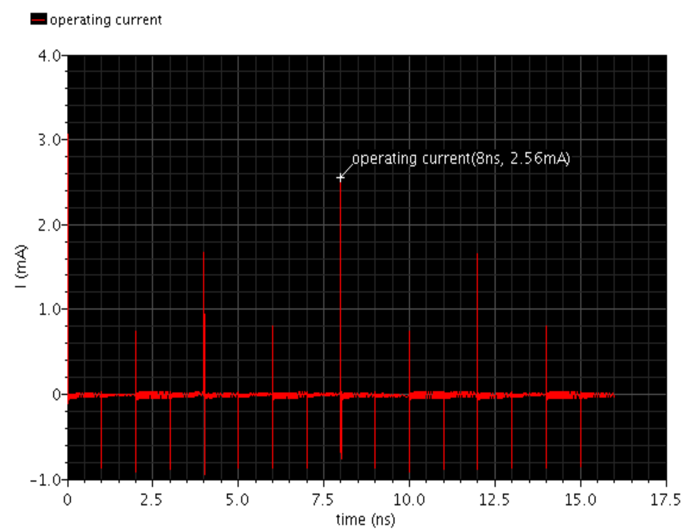

Fig.11(a) Operating current of 7T SRAM array

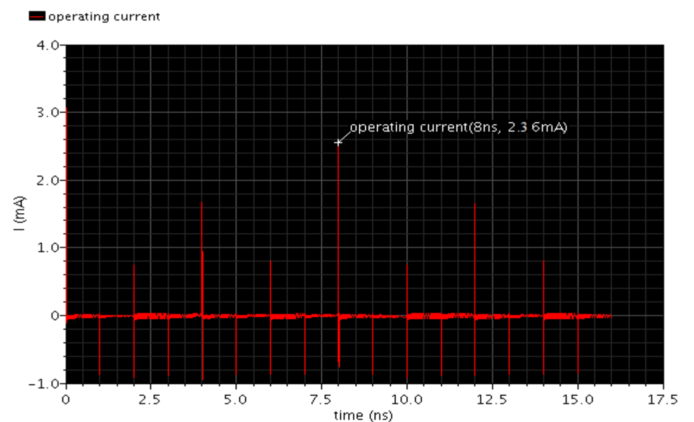

Fig.11(b)Operating current of 7T SRAM array using body biasing

E. Efficiency:

Efficiency in general describes the extent to which time or efforts are well used for the intended task or purpose. Quantitatively determined by the ratio of output to the input. Here estimated write efficiency for 16 bit array is 97.20%, and Read efficiency is 99.95% that shows how effectively the circuitry works[20].
Write efficiency noted for Array with body biasing is 99.93%, and read efficiency is 99.95%.

V. SIMULATION RESULTS:

In this section, we present simulation results on the leakage Current savings, Write and Read delay, and dynamic current of the above leakage power reduction technique, based on the UMC 45 nm CMOS process using cadence virtuoso tool is given in TABLE I.

TABLE I

Parameter	16bit SRAM array	16 bit SRAM array with body biasing tech.
Supply Voltage	0.7V	0.7V
Operating Current	2.565mA	2.362mA
Operating Power	11.89µW	11.69nW
Dynamic current	9.61µA	7.372µA
Dynamic power	742.2nW	389.1nA
Write Delay(27°C)	14.61ns	174.6ps
Read Delay(27°C)	15.05ns	265.5ps
Leakage current(27°C)	14.44nA	12.39nA
Leakage Power	1.347pW	881.7fA
Efficiency	97.20%	99.93%

VI. ACKNOWLEDEMENT:

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VII. CONCLUSION:

Static random access memory standby leakage power has become a major issue in modern low power SOC devices with technology scaling. This article summarizes the existing leakage reduction technique, i.e. body biasing scheme. We have also compared body biasing array with simple7T sram array them based on simulation results and they have demonstrated that different technique have different advantages and disadvantages. In a word body biasing scheme show greater leakage suppressing capability, and reduce delay also. As a result, SRAM cell optimization must be seeking a tradeoff between power consumption and device performance.

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