Design and Modelling FinFET Based on SRAM Cell

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***Abstract*- The limitations of scaling SRAM due to intrinsic variations and leakage control issues in bulk-Si MOSFETs. Two types of SRAM cells, six-transistor (6-T) and four-transistor (4-T) are presented and compared in terms of design tradeoffs. The passage suggests that 6-T and 4-T SRAM cells based on FinFET technology and designed with built-in feedback can significantly improve the cell static noise margin (SNM) without area penalty.**

The passage also states that a 6-T FinFET-based SRAM cell with built-in feedback can achieve up to a 2x improvement in SNM. Additionally, a 4-T FinFET-based SRAM cell with built-in feedback can achieve sub-100pA per-cell standby current and offer similar improvements in SNM as the 6-T cell with feedback. These features make the 4-T Fin FET-based SRAM cell attractive for low-power, low-voltage applications.

In summary, the passage highlights the challenges in scaling SRAM due to intrinsic variations and leakage control issues in bulk-Si MOSFETs. The passage suggests that FinFET-based SRAM cells with built-in feedback can significantly improve the cell static noise margin without area penalty and offer low standby current, making them attractive for low-power, low-voltage applications.

Keywords: FINFET, Transistors, SRAM Cell, Bulk -Si MOSFET.

I. INTRODUCTION

The challenges of scaling SRAM cells in modern chip designs. SRAM arrays currently occupy a significant portion of the chip area, and as memory demands continue to increase, memory density must scale alongside logic. However, conventional 6-T SRAM cells face challenges in scaling due to increased transistor leakage and parameter variation.

As MOSFETs are scaled down to the nanoscale regime, statistical dopant fluctuations, oxide thickness variations, and line-edge roughness contribute to increased variability in transistor threshold voltage (Vt), leading to increased spread in on- and off-currents. To limit static power dissipation in large caches, a lower supply voltage can be used [7], but this compromises cell stability, measured as the static noise margin [8].

In summary, the passage highlights the challenges of scaling SRAM cells due to increased transistor leakage and parameter variation caused by scaling MOSFETs to the nanoscale regime. To limit static power dissipation in large caches, a lower supply voltage can be used, but this compromises cell stability, measured as the static noise margin. These challenges must be overcome to continue scaling SRAM cells and increase memory density in modern chip designs.

The passage introduces the FinFET transistor structure as an alternative to the bulk-Si MOSFET structure for improved scalability in modern chip designs [9]. The FinFET structure utilizes a Si fin as the channel/body, with the gate electrode straddling the fin. The fin width is the effective body thickness, and the fin height is the effective channel width. In the ON state, current flows between the sources to drain end to end the gated sidewall surfaces of the Silicon fin

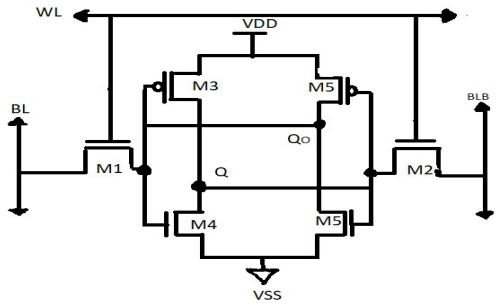

Figure 1: Schematic of a conventional 6-T SRAM cell.

The FinFET structure is intended to suppress short-channel effects by applying a thin body, i.e., by making the fin very thin, less than the channel length. Heavy channel doping is not required for short-channel effect control, minimizing variations due to statistical do pant fluctuation effects.

The gates on either side of the fin can be electrically isolated to permit for independent operation. In double-gate (DG) operating mode, the two gates are biased together to switch the FinFET on/off, while in back-gate (BG) operating mode, they are biased independently. BG operation offers dynamic performance tunability, which can be leveraged to improve trade-offs in SRAM design.

The passage then analyses the design constraints and trade-offs for a conventional 6-T SRAM cell and shows how its design can be optimized to meet noise margin and power specifications. The challenges for bulk-Si SRAM technology scaling are discussed, and FinFET-based SRAM cell designs are presented. Built-in feedback is shown to be an effective technique for achieving dramatic improvements in the cell read margin while providing very low standby power consumption.

II. 2.6T SRAM DESIGN TRADE

2.1 Area vs. Yield

Indeed, the tradeoff between functionality and density is a crucial consideration in memory array design. Increasing the size of the transistors in a memory cell can increase the noise margins, which improve cell stability and functionality, but it also increases the cell area and reduces the overall density of the memory array. Conversely, reducing the size of the transistors can increase density but may compromise functionality and stability due to increased leakage and parameter variations. Therefore, memory array designers must carefully balance these factors to achieve the desired performance within the given area constraints.

2.1.1 Hold Margin-

As the supply voltage is decreased during standby mode, the PMOS load transistor (PL) must compensate for the sub-threshold and gate leakage currents of all the NMOS transistors connected to the storage node VL (Figure 1). This becomes more challenging in recent technology nodes due to the increase in gate leakage and degradation in ION/IOFF ratio [7]. Therefore, designing robust low-power memory arrays becomes increasingly difficult.

Static noise margin (SNM) is an important metric for measuring the hold stability of an SRAM cell in standby mode. It represents the minimum voltage disturbance that can cause the cell to flip its stored value. The SNM is determined by the voltage difference between the voltage at which the cell is stable and the voltage at which it becomes unstable [8]. It is commonly quantified by the length of the side of the maximum square that can fit inside the butterfly curves formed by the cross-coupled inverters. A higher SNM means that the cell is more stable and less prone to errors during standby.

2.1.2 Read Stability Margin-

During a read operation, the cell SNM is reduced due to the reduced gain in the inverter transfer characteristic caused by the parallel operation of AXR and PR [7]. This reduction in SNM makes the cell more vulnerable to noise during a read access. To increase the read margin, the pull-down transistor can be upsized, but these results in an area penalty. Alternatively, the gate length of the access transistor can be increased to increase the WL delay, but this would hurt the write margin. Therefore, a trade-off must be made between read stability and write margin.

2.1.3 Write Margin-

The write margin represents the level of noise immunity during a write operation, and it is measured as the maximum voltage that can be applied to BLC without causing a change in the cell state. To improve the write margin, the access transistor's width-to-length (W/L) ratio can be increased, which reduces the voltage divider's effect and allows a higher voltage to be applied to VL before it crosses the inverter's trip point. However, increasing the W/L ratio of the access transistor can adversely affect the read stability, which requires careful trade-offs between the read and write margins. Similarly, minimizing the size of the pull-up device (AXL) reduces the write margin but also reduces the cell's power consumption during writes.

2.1.4 Access Time

In a write operation, the voltage divider formed by AXL and PL pulls the storage node VL to a voltage level that is lower than the trip point of the inverter formed by PR and NR. When the voltage level of VL is below the inverter trip point, a successful write operation is achieved, and the cell state will flip almost instantaneously due to the positive feedback in the cross-coupled inverters. However, if the write operation cannot be completed before the WL is lowered, the write access fails.

In the pre charged bit-line architecture, the bit-lines are pre charged to a voltage level before a read operation. During the read operation, the voltage on one of the bit-lines will be pulled down to a lower level based on the state of the memory cell being accessed. The voltage difference (ΔV) between the bit-lines is then sensed by a sense amplifier, which amplifies the voltage difference to logic high or low level. If the voltage difference is not sufficient to trigger the sense amplifier before the WL is discharged, a read failure occurs. Therefore, a successful read access occurs if the required voltage difference (ΔV) can be developed before the WL is discharged [10].

2.2 Power-

On the other hand, using higher transistor threshold voltages can help reduce leakage without significantly impacting cell area. However, this comes at the cost of decreased drive current, which can negatively impact performance. In addition, higher threshold voltages can also reduce the cell stability, especially during read operations. Therefore, a careful balance must be struck between leakage reduction and performance/stability considerations when designing low-power SRAM arrays.

Other techniques for leakage reduction in SRAM arrays include power gating, where power is completely shut off to idle memory blocks, and dynamic voltage and frequency scaling (DVFS), where the supply voltage and frequency are reduced during idle periods. These techniques can significantly reduce standby power consumption, but come with their own set of design challenges and overheads.

The use of higher threshold voltages can help to improve the read and write margins, but it can also negatively impact the access time due to the lower read current. It is also important to note that high threshold PMOS loads tend to decrease the inverter trip point [5], while high threshold NMOS pull-down devices tend to increase it. Because the current heavy ability of the NPD is larger than the PMOS load, growing the threshold voltage of the NMOS transistors tends to have a powerful impact on the trip voltage, resultant in greater read and write margins.

Typically, the maximum standby power of the memory array sets a lower limit for the Vt in a given process, and then the margins are maintained by setting the supply voltage sufficiently high.

Using sleep transistors adds additional circuitry to the memory array, which increases the overall chip area and reduces the memory density. Body biasing can also be used to reduce leakage by adjusting the threshold voltage of transistors based on their operating conditions. However, this technique requires additional circuitry to generate the body bias voltage, which again increases the chip area and reduces the memory density. Additionally, body biasing can affect the stability of the memory cells, so it needs to be carefully designed and optimized.

2.3 Challenges for Scaling Bulk-Si SRAM-

As MOSFETs are scaled down to the sub-20nm regime, the control of short-channel effects (SCEs) becomes increasingly difficult. To control sub-surface leakage currents, heavy channel doping (>1018 cm-3) and heavy super-halo implants are required, which can severely degrade carrier mobilities due to impurity scattering and a high transverse electric field in the on-state. The increased depletion charge density also results in a larger depletion capacitance and hence a larger sub-threshold slope, which further degrades the on-state drive current for a given off-state leakage current specification. Moreover, off-state leakage current is enhanced due to band-to-band tunneling between the body and drain, and Vt variability caused by random do pant fluctuations becomes another concern for nanoscale bulk-Si MOSFETs.

Indeed, as technology scales down, the variability in critical dimensions and other process parameters increases, which can impact the stability and performance of memory arrays? This can result in the need for larger cell sizes or other circuit design techniques to improve yield and stability. As mentioned, segmentation is commonly used to speed up arrays, where the array is divided into smaller sub-arrays that can be accessed independently. This can help reduce wire delays and improve performance. However, it can also increase the overhead area of sense amplifiers and other circuitry, which can impact the overall density of the memory array. Therefore, careful design trade-offs must be made to balance performance, yield, and density in embedded, low-power memory applications.

III. FINFET DESIGN FOR SRAM

FinFET-based SRAM cells have several advantages over bulk-Si MOSFET SRAM cells, including enhanced performance due to reduced SCE, higher carrier mobility, negligible depletion charge and capacitance, lower parasitic device capacitance, and reduced Vt variations due to statistical dopant fluctuation effects. These benefits ultimately lead to improved power consumption, performance, and stability in FinFET-based SRAM arrays.

IV. FINFET DESIGN AND MODELING

It is stated that mixed-mode device simulation using the drift-diffusion model for carrier transport and the density gradient model is employed to simulate the DC transfer characteristics of SRAM cells under different biasing conditions[9]. However, the simulation does not take into account high-field transient velocity overshoot effects, and therefore the drain current values may be underestimated. However, the simulation is still valid in determining the trends and differences between device technologies and their impact on SRAM noise margins, as they depend on the relative strengths of two transistors and not their absolute ION. Access time simulations were not performed due to the unreliability caused by the error in estimating ION together with unknown interconnects properties.

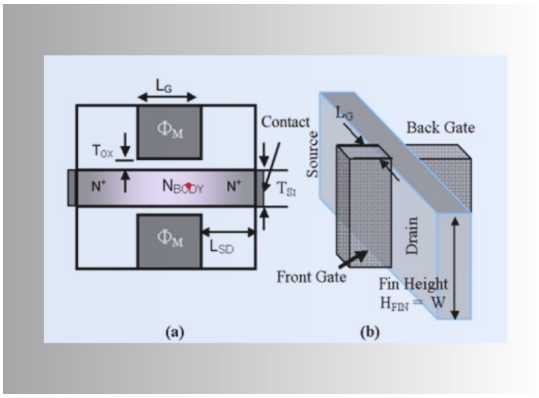

Figure 2: (a) Cross-sectional of double-gate MOSFET structure. (b) The gates of the FinFET can swing together in double-gated operation or back-gated operation.

It seems that the study we are referring to investigates the performance of FinFET and bulk-Si MOSFET transistor structures, focusing on the impact of short-channel effects and parasitic resistances and capacitances on SRAM cell performance. The study uses a mixed-mode device simulation approach that combines the drift-diffusion model and the density gradient model to account for quantum-mechanical effects in nanoscale MOSFETs. The results indicate that FinFETs exhibit improved performance over bulk-Si MOSFETs due to their intrinsic device structure and the better control of short-channel effects. The study also takes into account the effect of fin-sidewall surface orientation on FinFET performance [14].

The transistor structures used in this study are shown in Figure 2 and the key design parameters are summarized in Table 1. FinFETs fabricated on a standard (100) wafer have channels on the fin sidewalls that are oriented along (110) planes, for standard layouts. To capture the effect of fin-sidewall surface orientation on FinFET performance, the carrier flexibilities in Taurus [13] are calibrated using experimental data for the (110) surface [14].

4.1 FinFET SRAM Cell Designs-

4.1.1 Conventional Double gated (DG) Design-

The simulation results show that the read margin is sensitive to the strength of the pull-down transistor, as expected. However, the read margin improvement by size-ratio scaling is limited by increasing the bit-line capacitance (BL) as the cell size is reduced. The DG design also suffers from low write margin due to the limited voltage swing of the BL. These limitations can be overcome by employing segmented bit-lines and the virtual ground (VG) scheme [15-16]. In this scheme, the BLs are divided into segments, and the SRAM cells are divided into blocks. Each block of cells is connected to a BL segment and is accessed by a corresponding word-line (WL). By pre charging the BL segments to different voltages, it is possible to reduce the voltage swing on each segment, thus improving the write margin.

Table 1: Device parameters used for Taurus simulations

Parameters	FinFET	Bulk-Si
L_G (nm)	23	23
L_{SD} (nm)	25	25
T_{si}(nm)	16	1
T_{ox} (m)	1.1E-9	1.1E-9
S/D doping gradient (nm)/dec)	5	5
Channel Doping, N_{BODY} (cm)	10^{13}	$5x10^{15}$
Fin Height(H_{Fin}(nm))	31	-
V_{DD}(V)	1.1	1.1

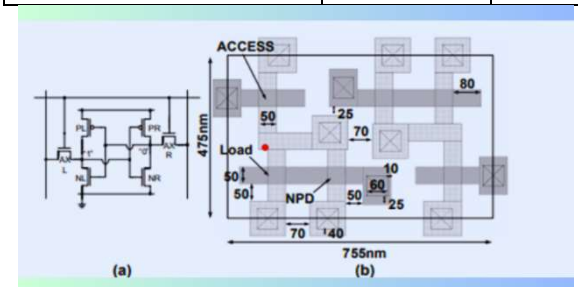

Figure 3: Circuit schematic (a) and layout (b) for a conventional DG 6-T SRAM cell. The outline specifies the area of one memory cell.

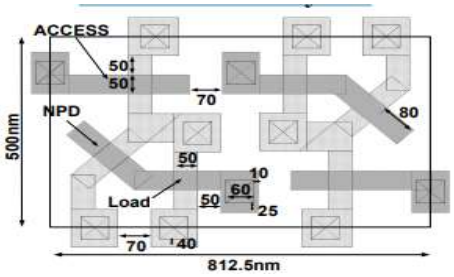

Figure 4: DG 6-T SRAM cell layout with rotated (100) NPD

This work proposes rotating the fins of FinFET-based SRAM cells to have the channel surface along the (100) plane in order to increase the effective cell β-ratio and improve the cell read margin. This is unlike cell designs in planar bulk-CMOS, where it is not as easy to fabricate transistors with channels along different crystal planes. By rotating the fins by 45° for the (100) fins,(figure 4) transistors with channel surfaces along both (110) and (100) planes can be easily fabricated. However, this may be lithographically more challenging and may result in enhanced process variations as a trade off.

Increasing the size of the pull-down transistor (figure 5) can lead to greater improvements in read margin, but this comes at the cost of increased area and power consumption. On the other hand, increasing the length of the access transistor has less impact on cell area but can result in slower access times due to increased WL capacitance and decreased read current. So there is a trade-off between read margin improvement and area/power/access time considerations.

In Figure 6, the simulation results for the butterfly curves of two different SRAM cells are compared: a 6-T bulk-Si MOSFET-based SRAM cell and a 6-T FinFET-based SRAM cell with 1-fin. The conventional DG 6-T FinFET-based SRAM with 1-fin achieves a 22% improvement in the read SNM compared to its bulk-Si-based counterpart with a β-ratio of 1.5. The simulation results also show that rotating the pull-down transistor can further improve the read SNM by 15% with a 13.3% area penalty, while upsizing the pull-down transistor by 1-fin can further improve the read SNM by 36% with a 16.6% area penalty. To reduce leakage and recover read/write margin, higher threshold pull-down devices were used in the FinFET designs by floating the gate work function of the NMOS and PMOS devices to 4.75eV. This resulted in improvements in SNM as shown in Figure 6c. However, it is important to note that a higher Vt bulk-Si device might not necessarily translate to lower leakage due to band-to-band tunneling.

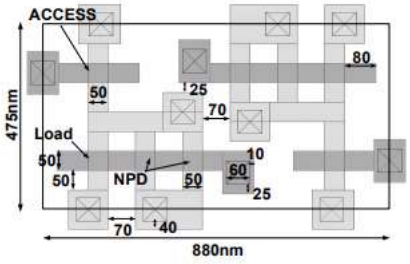

Figure 5: 6-T SRAM cell layout with 2-fin pull-down FETs

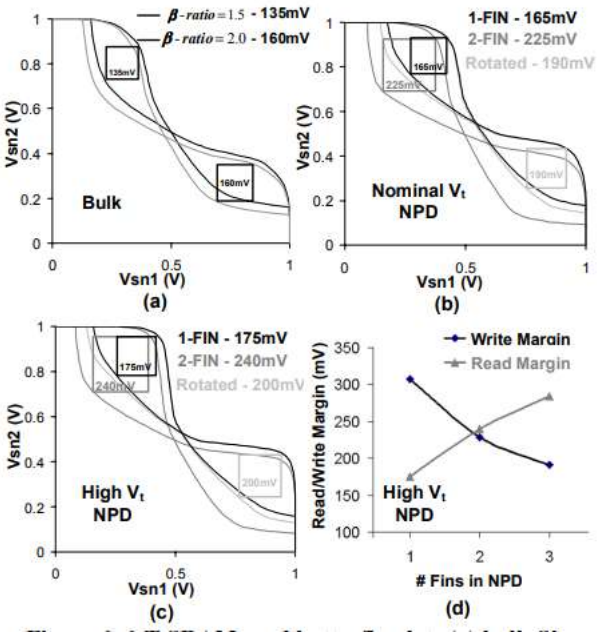

Figure 6: 6-T SRAM read butterfly plots (a) bulk-Si MOSFET SRAM cell with β-ratio = 1.5 of black, 2.0 of gray and (b-c) FinFET-based SRAM cell with 1-fin (black), 2- fins, and rotation. (d) Impact of adding fins to the NPD on the read and write-margins.

Strengthening the pull-down devices by adding fins or rotating the channel surface plane can improve the read margin but can also reduce the write trip voltage, which in turn can lead to a reduction in the write margin. Figure 6d summarizes the effects of inserting extra fins on both the read and write noise margins

4.1.2 Back-Gated (BG) Designs

Back-gate biasing is a technique used to dynamically control the threshold voltage (Vt) of a MOSFET by applying a voltage to the substrate (back gate)[17]. This technique remains effective with thin-body MOSFETs, which are used in FinFETs, even as the transistors scale down in size. Adaptive body biasing [18], which is another technique for dynamically controlling Vt, becomes less effective with scaling of bulk-Si MOSFETs.

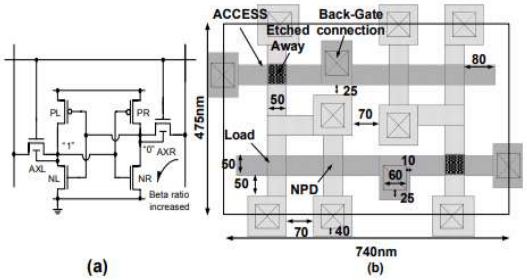

Figure 7: Circuit schematic (a) and layout (b) for a 6-T SRAM cell with back-gate connections to provide dynamic feedback.

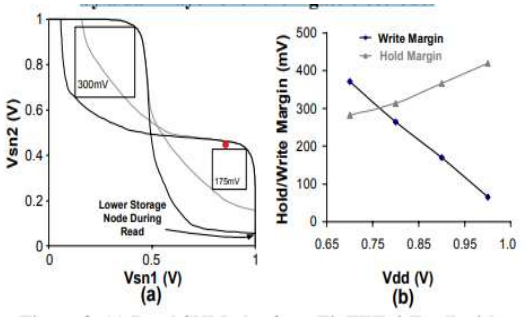

Figure 8: (a) Read SNM plots for a FinFET 6-T cell with feedback. (b) Impact of cell supply on write margin and standby SNM

This technique is known as back-gate feedback (BGF) and it can improve the read margin of FinFET-based SRAM cells. By selectively decreasing the strength of the access transistor using the back-gate of the corresponding transistor, the β-ratio can be increased during the read cycle, leading to an improvement in the read margin. The feedback is achieved by connecting the storage node to the back-gate of the access transistor. If the deposited bit is a "0", the back-gate of the consistent access transistor is biased at 0V, reducing its strength. The storage node in the 6-T design with feedback stays closer to VSS than the conventional design, which gives the BG access transistors more gate overdrive. This results in a 71% read margin improvement over the conventional design.

Lowering the cell supply voltage during write can significantly improve the write margin of the 6-T SRAM design with feedback. The long AR cell layout allows column-based biasing, which allows the cell supply voltage to be selectively lowered only for the column covering the cell under write access. This reduces contention between read- and write-optimization and replaces it with a contention between hold- and write-margins. This approach provides a bigger window for optimization, and high read and write margins can be independently achieved. Figure 8b summarizes the improvement in write margin due to reduced cell supply and the consistent impact on the hold SNM.

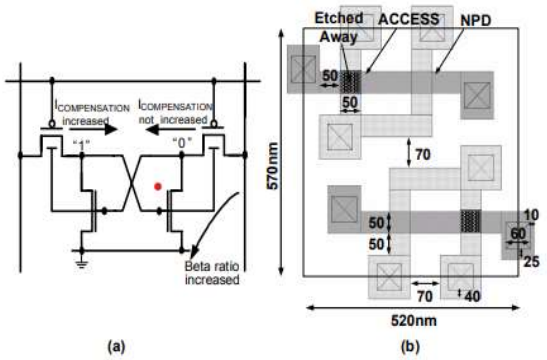

Figure 9: Circuit schematic (a) layout (b) for a 4-T SRAM cell with back-gate connections to provide dynamic feedback.

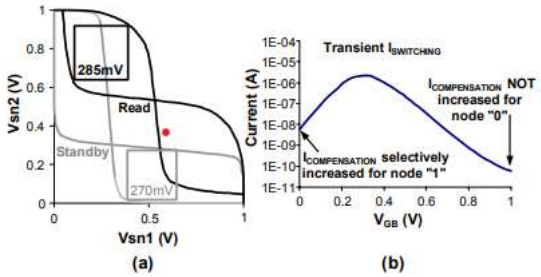

Figure 10: (a) SNM plot for a 4-T cell with feedback during standby for gray and read for black. (b) Using dynamic feedback, ICOMPENSATION is selectively increased to compensate "1" storage node.

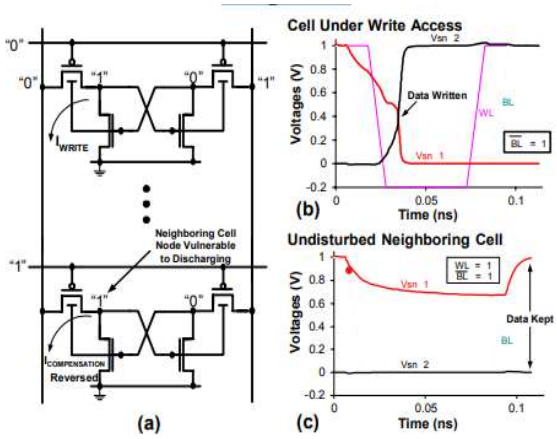

Figure 11: (a) 4-T SRAM neighboring cell write upset set-up. (b) Write simulation with word line swing of –200mV to 1 V. (c) write simulation of uninterrupted neighbouring cell.

4.1.3 4-T Cell Design with Dynamic Feedback-

In conventional 4-T SRAM cell designs, both PMOS access transistors are used to compensate for the leakage currents[18] in the pull-down transistors during standby, even though compensation current is only needed for the "1" storage node. This results in high power dissipation as both PMOS access transistors draw currents from the bit-lines.

The dynamic control of the PMOS threshold voltage (Vtp) allows for the selective adjustment of the compensation leakage current in the 4-T SRAM design. By cross-coupling the storage node to the back-gate of the access transistor on the opposite side, high compensation current can be selectively injected only into the "1" storage node, resulting in higher effective β-ratio for the cell design. Additionally, the access transistor connected to the "0" storage node is made weaker by back-gate biasing it with the "1" storage node, resulting in a further improvement in read margin. Overall, this approach achieves a significant improvement in read margin on top of a considerable area savings compared to the conventional DG 6-T design.

Compared to the conventional DG 6-T design obtainable earlier, the 4-T design with feedback reaches a 63% improvement in read margin on top of a 17.6% area savings.

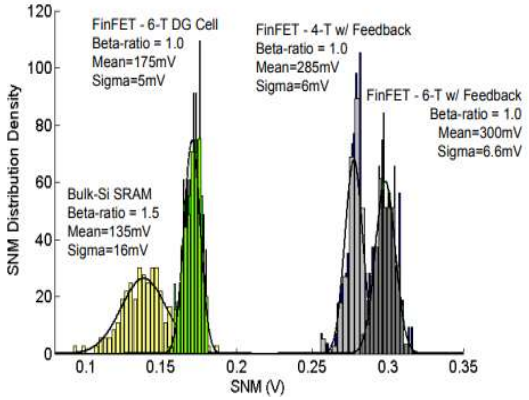

Figure 12: Impact of process variations on SNM. Cell designs with dynamic feedback have improved noise margin than the standard 6-T DG-SRAM. Do pant induced variations because greater SNM spreads in the bulk devices.

In the conventional 4-T SRAM cell design, a potential issue arises when a neighboring cell (sharing the same bit-line) is being written, which can cause a bit-flip in the current cell being accessed. This happens because the directions of the compensation currents can be reversed in the cells connected to the same bit-lines when the bit-lines are set according to the data to be written. This issue can be addressed by ensuring that the PMOS devices can only pull a "1" storage node down to a certain voltage, which is higher than the NMOS threshold voltage. By employing high-Vtp PMOS and low-Vtn NMOS devices, neighboring cell write upset can be alleviated. High-Vtp PMOS devices tend to be relatively weak, so PMOS drive current can be increased to improve write margin by using a negative word-line bias voltage.

4.1.4 Process-Induced Variations-

Process-induced variations in device parameters cause V_t variations resulting in spread in SRAM SNM distributions. In order to examine the impact of fluctuations in device parameters such as L_G and T_{Si} in FinFETs ($3\sigma L_G = 3\sigma T_{Si} = 10\% L_G$) and the impact of random dopant variations in bulk devices [20]. The impact of statistical variations in device parameters in FinFETs and bulk devices on the cell read margin is illustrated in Figure 12.

4.2 Array Design Issues-

4.2.1 Sleep-mode features

It seems like the passage you provided is discussing various techniques to reduce leakage current in 4-T SRAM designs while maintaining high standby SNM. One technique mentioned is the dynamic control of PMOS threshold voltage (Vtp), which selectively adjusts the compensation leakage current and increases the effective β-ratio for the 4-T SRAM cell design.

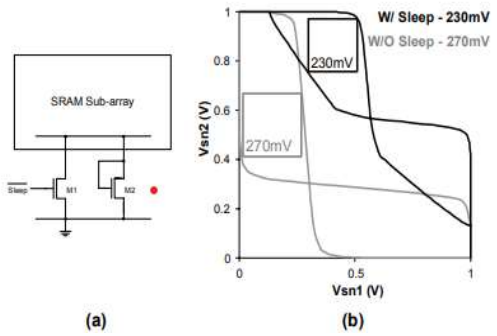

Figure 13: (a) Gated VSS leakage reduction scheme for the 4-T SRAM design. (b) Standby SNM plots for the 4-T SRAM cell with and without gated VSS leakage reduction.

Another technique mentioned is the integration of NMOS sleep transistors into each sub-array to reduce leakage during standby mode, which incurs a small degradation in cell standby SNM. The passage also discusses the impact of process-induced variations in device parameters on SRAM SNM distributions and the use of Monte Carlo simulations to analyze this impact. Finally, the passage compares the simulated cell standby currents for 4-T and 6-T FinFET-based SRAM designs, which can achieve less than 0.2nA/cell and 80pA/cell, respectively, while maintaining a high standby SNM.

V. CONCLUSION

Based on the analysis using mixed-mode Taurus simulations, the FinFET-based SRAM cells outperform SRAM cells designed in planar bulk-Si MOSFETs. Specifically, conventional FinFET-based 6-T DG designs with high Vt provide a read SNM of 175mV, which is a 30% improvement over the bulk-Si MOSFET SRAM cell with a β-ratio of 1.5. Moreover, by utilizing built-in feedback to dynamically adjust transistor strengths, the cell SNM can be further improved by 71% with little performance and no area penalty, achieving 300mV SNM while keeping standby leakage current below 0.2nA/cell.

In addition, the 4-T FinFET-based SRAM cell with built-in feedback can achieve more than 17% area reduction with 285mV SNM during read and 230mV SNM during standby, while providing less than 80pA/cell of leakage current during standby. This makes it highly attractive for high-density, low-power cache memory applications.

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