Design And Analysis of Low power SRAM Cell Using Power gating CMOS Technology

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***Abstract*— At present time demand of low power circuits are most popular. This circuit used as the scaling increase the leakage powers increases. So for removing these leakage problem we are using many types of power gating techniques in SRAM cell and to provide a better power efficiency. In this paper by using 6T SRAM cell design a power gated circuits. We are going to display the comparison results between different nano-meter technologies. "Empyrean Aether" tool are used for simulations & circuit design. In all simulation have been carried out at 180 nm technology.**

***Keywords*— CMOS, Leakage Power, Power Gating, VLSI.**

I. INTRODUCTION

In recent here we have seen the decreasing the continuously features size and corresponding increasing chip density and operating frequency have made power consumptions a major concern in VLSI design. In nano scale technology, SRAM becomes increasingly vulnerable to noise sources. For demanding low power consumption during active operation, The major role of supply voltage which is useful. The reliability of SRAM is depends on the low supply voltages. In this paper, We will emphasize SRAM read and write margin analysis and compare the different SRAM cells configuration on the basis of stability.

The growing need for portable communication devices and computing system has increased the need for optimization of power consumptions in the chip now we will see some smart technology which is use for reducing power and give high speed performance.

II. SRAM

6T SRAM cell can be designed by using 2 PMOS and 4 NMOS transistor as shown in fig (a). It consist of two cross coupled inverters and two acess NMOS transistor M5 and M6 . These two cross coupled inverters, which are connected bach to back, are used for storing one bit of information at a time (either 0 or 1). The two additional acess transistor is used to control access to a storage cell during read and write operation.this access two enable by the word line (WL) which control these two access transistor M5 and M6 which, in turn , control weather the cell should be connected to the bit lines, bit and bit bar[1]. They are used to transfer data for both read and write operations. The value of bit and bit bar is inverted . when bit is high then bit bar will be zero and vice versa. widely used as criteria of stability. SNM is basically minimum DC noise voltages with the help of flip cell state. MT CMOS is an important technique for power dissipation. It is basically works on the high speed and reducing the leakage power.

Power dissipation can be reduced by scaling the supply voltages threshold voltage Vt results in exponential increase of the subthreshold leakage current [2], [3].

III. 6T SRAM CELL STABILITY

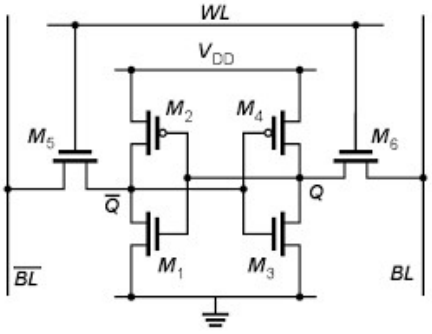

Fig (a): 6 T

The 6T SRAM cell can be designed with the help of PMOS and NMOS transistors. PMOS has two transistors and NMOS has a four transistors. shown in fig a. according to fig two cross coupled inverters and two access NMOS transistors M5 and M6 . These two cross coupled invereters, which is

connected back to back , are used for storing 1 bit of information at a time (either 0 or 1) . the two additional acess transistor for storage cell during read and write operation. This access to the cell is enabled by word line (WL) which controls these two access cell should be connected to the bit lines, bit and bit bar [1]. They value of bit and bit bar is inverted . when bit is high then bit bar will be zero and vice versa.

Here PMOS and NMOS both are used in cross coupled phenomena.

Three modes of operation is enrgised is as following

a) Standby mode
b) Read mode
c) Write mode

IV. POWER GATING TECHNIQUE

This method is to reduce the leakage power. This technique is disconnecting the components in the circuit temporarily that are currently not in use. Basic implementation of power gating is to use an externally switched power supply and shut-off supply when required. In CMOS technique , CMOS switches are provide power to the circuit can be controlled. A major technique of power gating is to use sleep transistors to control the sub-threshold current [4]. In this paper, we have implemented a sleepy structure that merges stack technique and sleep transistor. Normal SRAM cells have lower threshold voltages but the sleep transistors have higher threshold voltages. Normally in PMOS and in NMOS, low leakage PMOS transistors are used as header switches to shut-off power supply Footer NMOS devices are also used to control power supply to the circuit.

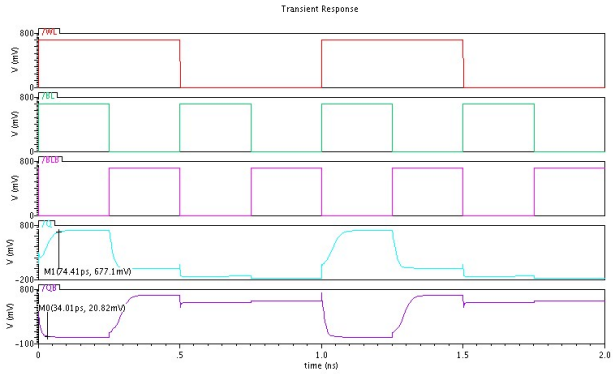

Fig (b) output wave form of 6T SRAM using power gating technique

V. MODIFED SRAM WITH POWER GATING TECHNIQUE

Power gating operated in CMOS circuited. In SRAM cell which have lower threshold voltage. But MT CMOS have multi threshold voltage which is very effective for reducing power. In MT CMOS there are two mode of operation either is active or sleep mode. In sleep transistor have higher threshold voltages. Which provide the decresing power with increasing speed and techniques. Now in 6T SRAM cell will modified structure as fig (c)

According to the fig (c) here we have added two NMOS transistor connected in series. These transistor is to modified the 6T SRAM cell. With the help of these modification the leakage current is reduced with reducing power also. So in advance terminology of power gating is modified. Here the role of MTCMOS is to provide multi threshold voltages there SRAM performed and operation of power gating is done.

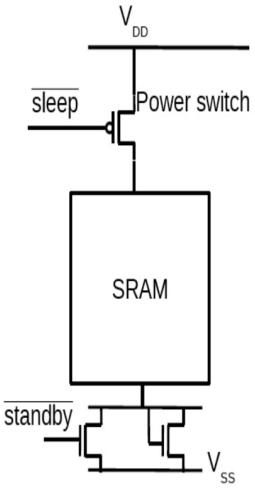

Fig. (c) Modifed SRAM with Power Gating Technique

VI. PERFORMANCE ANALYSIS AND RESULT SIMULATION

In this paper, We have performed simulation of our base 6T SRAM CELL and modified 6T SRAM CELL using Power gating technique on empyrean aether tool and SPECTRE simulator at 180nm technology.

A. ACTIVE POWER

Supply	Base 6T SRAM CELL		Modified 6T SRAM cell	
Supply and temperature	0.7V	27^0C	0.7V	27^0C
Active power (N w)	3.58	3.58	1.35	1.35

Active power dissipated by the circuit at operation condition. Here we will calculate active power at 180nm technology. The active power includes both dynamic and static power. The active power consumption of CMOS circuit [7][8] is described by following equation-

$$Pactive = Pdyanamic + Pstatic \quad (1)$$

$$= Pswitch + Pshort + Pleak \quad (2)$$

$$P = \alpha_{D-1} X C_1 X F_{clock} X V^2_{dd} + I_{short\text{-}circuit} X V_{dd} + I_{leakage} X V_{dd} \quad (3)$$

Where α_{D-1} =Probability, C_1=Load capacitance, F_c=clock frequency, V_{dd} =Power supply, I_{short} =Short circuit current,

I_{leak}= Leakage current. As shown in table here we will modified 6T SRAM cell using MT CMOS Technique.

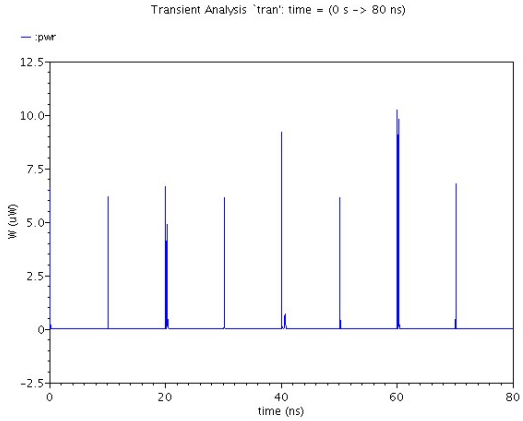

Fig. (f) Active power of 6T SRAM cell

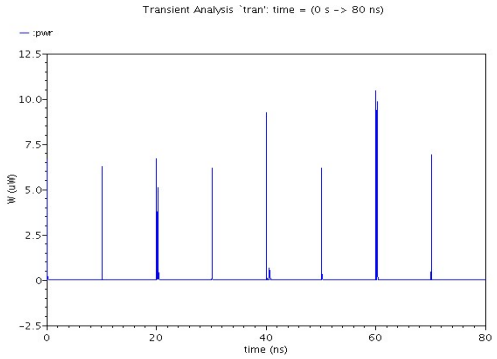

Fig (g) Active power of Modified 6T SRAM cell

Table 2 : Active power dissipation of 6T SRAM cell

Circuit	Base 6T SRAM cell		Modified 6T SRAM cell	
Supply and Temperature	0.7 V	27° C	0.7 V	27°C
Active power (nW)	3.58	3.58	1.35	1.35

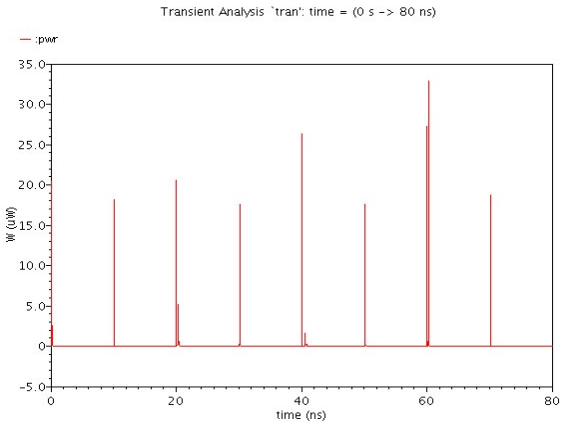

Fig (h) Active power dissipation of 6T SRAM cell

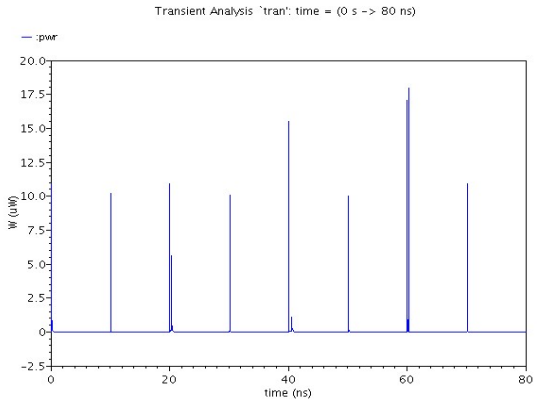

Fig (i) Active power dissipation of Modified 6T SRAM

B. STAND BY LEAKAGE CURRENT

This current operate when the cicuit is in idle mode. Here we connect the sleep transistor to the pull down network NMOS And to pull up network PMOS circuit. We measure the leakage current and power gatting using MT CMOS technique. The basic equation of leakage current is[9]

$$I_{Leakage}=I_{Sub}+I_{OX} \quad (4)$$

Where, I_{sub}=Sub threshold leakage current.

I_{ox} = Gate oxide current.

$$I_{Sub}= K_1We^{-vth/nvo}\ (1-e^{-v/vo}) \quad (5)$$

Where k1 and n is experimentally derived,W is gate width,Vθ is thermal voltage, n slope shape factor/ sub threshold swing coefficient,V_{th} is threshold voltage.

$$I_{ox}=K_2W(V/Tox)^2e^{-\alpha Tox/Vo} \quad (6)$$

Where K_2 and α are experimentally derived, Tox is oxide thickness. Stand by leakage current is measure. 7V voltage and 27°C temp. It is greatly 90% power gatting with modified 6T SRAM CELL using MT CMOS. In table 3 and 4. As shown various voltages and temperature.

- Table 3. STAND BY LEAKAGE CURRENT AND LEAKAGE POWER DUE TO VARIOUS VOLTAGES.

Voltage v	Leakage current		Leakage power	
	Base6T SRAM(n A)	Modified 6T SRAM (n A)	Base6T SRAM(n W)	Modified 6T SRAM (n W)
0.5	0.92	1.31	4.99	4.15
0.7	4.38	1.86	16.68	11.61
0.9	10.37.75	4.87	32.39	17.76
1.1	17.6	11.59	56.75	34.85
1.3	25.8	19.43	84.73	45.98

- Table 4. STAND BY LEAKAGE CURRENT AND LEAKAGE POWER DUE TO VARIOUS TEMPERATURE.

Temp. 0C	Leakage current		Leakage power	
	Base 6T (nA)	Modi. 6T (pA)	Base 6T (nA)	Modi. 6T (pA)
27	4.38	1.86	16.68	11.61
47	4.46	1.92	17.43	12.68
67	4.60	2.02	18.19	13.77
87	4.84	2.16	18.91	14.09
107	4.91	2.30	19.63	14.56

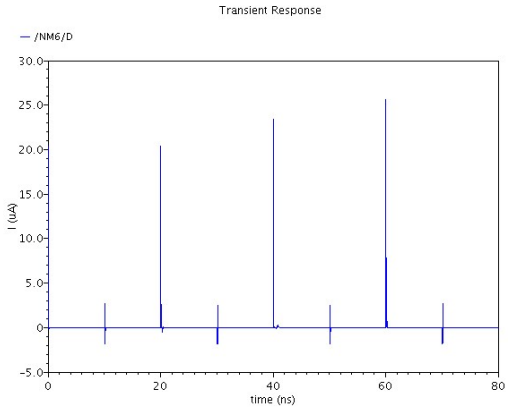

Fig (j) Stand by leakage current of 6T SRAM cell

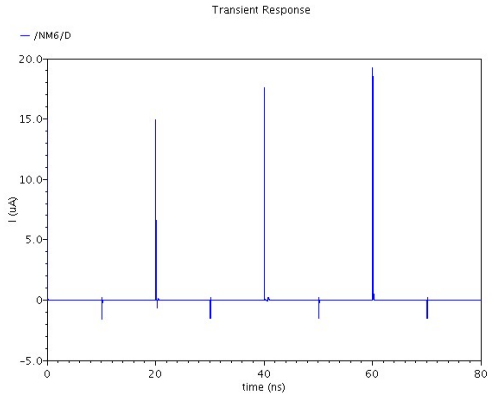

Fig (k) Stand by leakage current of Modified 6T SRAM cell

C. Stand by leakage power-

Stand by leakage power is measured at the time of idle mode. Leakege power is measured when the sleep transistor is off. The equation of leakage power is

$$P_{leakage}=I_{leakage}\,X\,V_{dd} \qquad (7)$$

Where P_{leak}=Leakage power,$I_{leakage}$=Leakage current and V_{dd} is supply voltage. According to the equation the power depends upon the leakage current and supply voltage.

- Table 3. STAND BY LEAKAGE POWER AND LEAKAGE CURRENT DUE TO VARIOUS TEMPERATURE.

Temp in 0C	Leakage current		Leakage power	
	base 6T SRAM (nA)	modified 6T SRAM (nA)	base 6T SRAM (nW)	modified 6T SRAM(nW)
27	4.38	1.86	16.68	11.61
47	4.46	1.92	17.43	12.68
67	4.60	2.02	18.19	13.77
87	4.84	2.16	18.91	14.09
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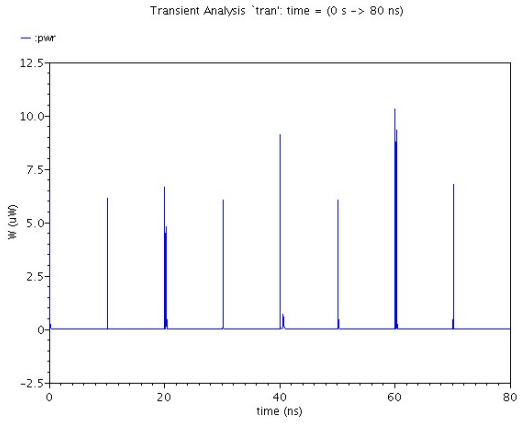

Fig (l) stand by leakage power of 6T SRAM cell

CONCLUSION

The Simulation result discussed above improve the read and write stability of SRAM which is increased the power dissipation and due to increase in area. The Stability performances of three SRAM cell topologies have been presented. As process technologies continue to advance, the speed of SRAM will increase, but devices will be more susceptible to mismatches, which worsen the static-noise margin of SRAM cells. Leakage power reduction has become one of the main optimization challenges for today some micron design. This paper describes about power gating and leakage power optimization technique is the main focus throughout this paper. The concept of sleep transistor is simple best sleep transistor design and implementation require optimizing all together the gate lan, width and body bias width overall opinion of effective leakage, drive, area and IR drop effect which are useful for this application.

In future the work can be extended by adding Multi-Vt technique along with the coarse grain to analyze how efficiently we can reduce leakage power.

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