Modification in 16:1 Muliplexer by Reversible Logic

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Abstract— **Reversible logic is widely advantageous in the field of researchers in instantly Reversible logic concept of digital circuit designing is gaining wide scope in the field of MEMS ,Control System, analog Computing, quantum computing, Digital signal processing, optical computing etc due to advantageous design for low power loss in digital circuits. In this paper we have a compact multiplexer circuit based on reversible logic apply different Reversible Logic gates is achieved on the In Compact circuit o finally generated the total no. of output. These circuits are efficient according to total number of gates apply in the logic circuit and for low power loss.**

Keywords— Reversible Logic, Gate, Multiplexer, Feedback Logic.

I. INTRODUCTION

An integrated circuit containing many identical cells which can be electrically programmed to become almost any kind of digital circuit or system is called as Field Programmable Gate Arrays (FPGAs) [1].Digital circuits were made of conventional logic gates. These gates were irreversible in nature. Reversible circuit designing is the way of todays digital circuit designing. In 1961, R. Landauer has shown that these conventional irreversible circuits dissipate some energy due to the information loss during the operation of the circuit [2]. After that in 1973, Benette has shown that this energy loss can be minimized or even removed if the circuits are designed usingn reversible gates [3].

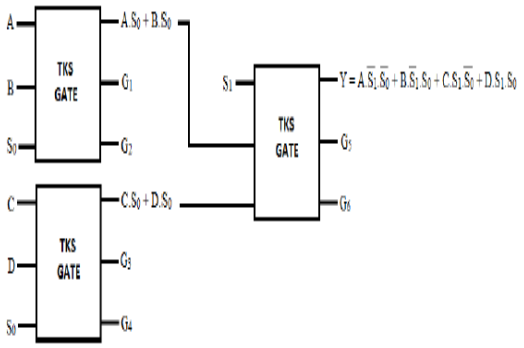


Fig. 1 . Schmatic Circuit of TKS

Where various output equations are given below-

$$E_1 = A.\bar{S}_0 + B.S_0$$
$$E_2 = C.\bar{S}_0 + D.S_0$$
$$Y = A.\bar{S}_1.\bar{S}_0 + B.\bar{S}_1.S_0 + C.S_1.\bar{S}_0 + D.S_1.S_0$$

In the approach 2 only one VSMT gate is used to design the 4:1 multiplexer. Input combinations applied toVSMT gate are by connecting A, B, C, D, S1, S0 i.e. input and selection line signals to the (A, B, C, D, E and F)

Where E1 and E2 are intermediate results of the circuit. Above design produces 6 garbage outputs using a total of 3 reversible gates. Now we will design the same 4:1 MUX circuit using the proposed 6X6 reversible gate i.e. VSMT gate. This circuit design approach 2 is shown in the figure below.

Here various output equations are as shown below-

$$Y = A.\bar{S}_1.\bar{S}_0 \oplus B.\bar{S}_1.S_0 \oplus C.S_1.\bar{S}_0 \oplus D.S_1.S_0$$

In the approach 2 only one VSMT gate is used to design the 4:1 multiplexer. Input combinations applied to VSMT gate are by connecting A, B, C, D, S1, S0 i.e. input and selection line signals to the (A, B, C, D, E and F) input lines of the reversible gate. Output Y is taken from the P output line of the gate. Other outputs of the VSMT gate produce the garbage outputs (G1, G2, G3, G4, G5). Here a total of 5 garbage output signals are produced by using single reversible gate. Comparison of these design approaches for 4:1 multiplexer is shown in table.

II. METHODOLOGY:

A. DESIGN OF 4:1 MUX USING REVERSIBLE GATES-

As explained in the earlier subsection, a 4:1 MUX has 2 selection lines and 4 input lines. The design of this multiplexer in reversible logic requires 3 TKS gates. Input signals areA, B, C, D and selection lines used are S1 and S0. The output variable is denoted by Y. The design approach 1 of the same using TKS gates only is shown in the diagram.

S. No.	Variable	Approach 1	Approach 2
1	Total Number of Reversible Gates used	3	1
2	Total Number of Garbage Outputs	6	5
3	1-Bit XORs	3	1

Fig .2. Table of varios Approach

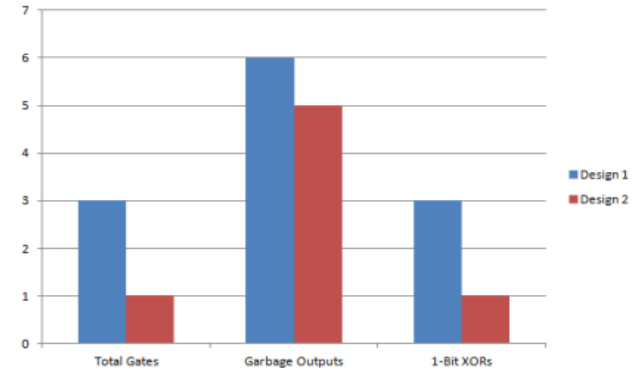


Fig .3. Various Approach using Bar Graph

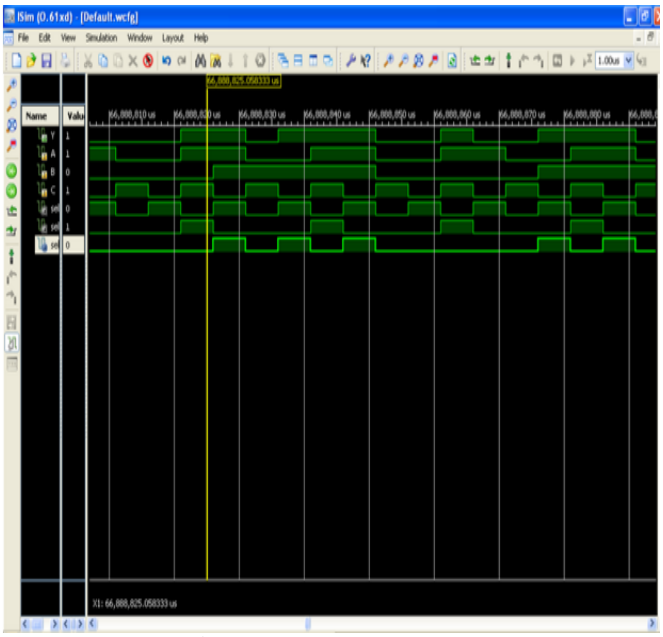


Fig .4. Simulation of 8:1 MUX

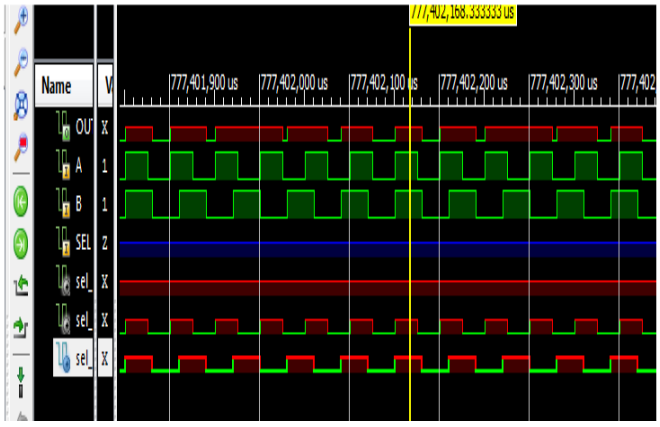


Fig.5: Simulation of 4:1 MUX

III. REVERSIBLE SYSTEM:

A. REVERSIBLE LOGIC:

Conventional logic is Reverse logic gates in which we have used (n: 1) Where n consist the number of input signals applied and 1 consist the single output generated by the gate. In Reversible logic gates of (n, n) logic gates represent the no. of output is equal to the no. of input. Where the number of input signals and the number of output signal both are equal to n. In analysis of conventional logic gates output signals are comparing to reverse logic. We have analysis that the no. of output is comparatively less in number of input signals. But in reversible gates input and the combination of output signal at any block can provide the value of input separately. According to this reason we have given the name is (n,n) gates, reversible Logic gates [4, 5, 6].

B. *BASIC REVERSIBLE GATES:*

There are different static logic of reversible (n,n) gates[7,8,9,10,11,12,13]. For designing multiplexer T gate [14] is the sufficient appropriate for reversible gate (3, 3) in. Its block diagram is shown in figure 1 and output equations are given below .

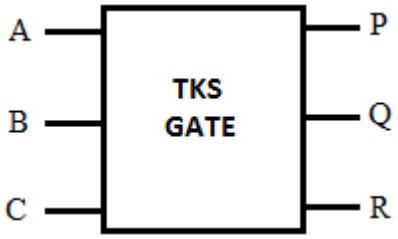


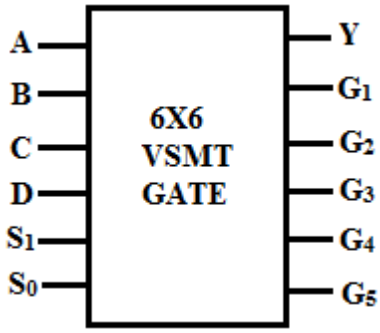
Fig.6. Schematic Block of TKS Gate

We have logic equation for above figure which are given below.

$$P = A.\bar{C} + B.C$$
$$Q = A \oplus B \oplus C$$
$$R = A.C + B.\bar{C}$$

A. . *PROPOSED REVERSIBLE GATE (VSMT GATE)*

VSMT is a new proposed (6,6) reversible gate.



B.
Fig.7. Schematic Block of 6*6 VSMT Gate

It consist of various s property of the reversible logic gates. These properties are given below.

(a) Number of inputs = Number of outputs is equal to the Number of inputs.
(b) The mapping between input and output using one to one bit .
(c) Using feedback with zero.
(d) Individual output bits are high for a total of half the number of total input combinations.

The block diagram of VSMT gate is shown in figure 2. Here input signals are A, B, C, D, E and F, whereas output signals are P, Q, R, S, T and U.

We are shown the the total of combinations of 64 input. In truthtable. In this gate we have generate the different output for each input VSMT gate is a combination of 6 input in reversible logic. We have given the research for VSMTgate to design multiplexer circuit .The purpose of used of multiplexer is that ,Increase the power signal of input in appropriate way.

C. *MULTIPLEXER CIRCUIT USING 8:1 MULTIPLEXER:*

In this circuit eight input data(ID0-ID7) three select lines(S2-So) and single output(Y).It also enable input Eo and provides both normal and inverted output. When Eo =0 the select input S2S1So will select one of the data input to pass through the output Y. When Eo =1 the multiplexer is disabled.

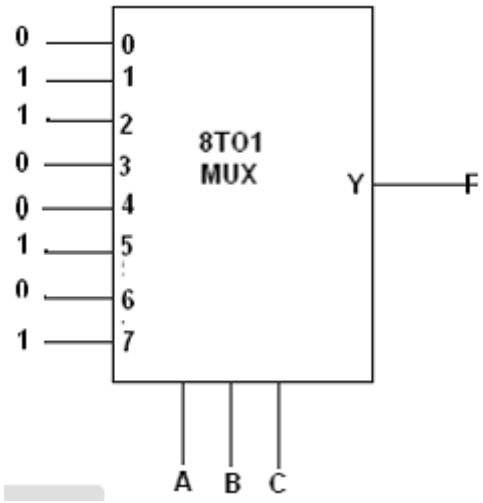


Fig.8. Block of 8:1 MUX

Inputs				Outputs
E0	S2	S1	So	Y
1	X	X	X	1
0	0	0	0	D0
0	0	0	1	D1
0	0	1	0	D2
0	0	1	1	D3
0	1	0	0	D4
0	1	0	1	D5
0	1	1	0	D6
0	1	1	1	D7

Fig.9. Truth Table of 8:1 MUX

IV. EXPERIMENTAL OUTPUT

We have shown in table, the value of different simulation using different value to be considered in the reversible circuit process of reducing design when we used for 4:1 multiplexer using reversible gate is designed with the help of the proposed VSMT gate. We have using only one reversible gate for design the circuit of 4:1 multiplexer The total number of garbage outputs produced are reduced to 5 as compared to 6 in the Latest technology.

V. CONCLUSION AND FUTURE SCOPE

Reversible logic is becoming the modern way of digital logic circuit designing. Here in this paper we have designed reversible circuits for 4:1 multiplexer. The optimized circuits are achieved with help of a proposed reversible gate i.e. VSMT Gate, which is a (6, 6) reversible gate. These designs can be furtherexpanded to achieve the reversible circuits for various other functions and devices. As multiplexers are the basic building blocks of FPGA boards. These proposed multiplexers with reversible gates will help the researchers to employ these FPGAs with reversible gates in low power logical design applications.

ACKNOWLEDGEMENTS

It gives me immense pleasure and satisfaction to express my Heart-felt gratitude to my guide Mr. Samir Mishra (IIT KGP) for providing me with excellent guidance and constant encouragement throughout my paper. A wonderful work place provided by advanced VLSI lab in Rama University, Kanpur.

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