Design and Analysis of Multi-Threshold CMOS 14T Full Adder using 180nm

Arvind Nigam
M.Tech. Scholar, Rama University, Kanpur
arvind_nigam@rediffmail.com

Raghvendra Singh
Dept. of ECE, Rama University, Kanpur
Raghav.raghvendra7@gmail.com

***Abstract*- In nanometer regime, the stand by leakage power and ground bounce noise are becoming most important parameter to kept in consideration are compactness and power which affects the performance usefulness of any VLSI circuits . Full Adder is the basic components of arithmetic and logic units of microprocessors. Improvement of this circuit would impart a greater impact on the performance of large systems where it has been employed. To improve the power consumption of the Full Adder the 14T structure has been utilized with MTCMOS technique at 180nm technology. In this paper, we have proposed a modified 14T full adder based on PTL using multi-threshold CMOS technique. Here we use forward body biased multimode (MTCMOS) technique to evaluate standby leakage current, power and ground bounce noise. The forward body biased (FBB) multimode MTCMOS technique has been implemented on conventional 14T full adder circuit with 180 nm technology parameters for simulations. All simulations have been carried out using Empyrean Aether in a 180 nm technology at various voltages and temperatures.**

Keywords- Ground bounce noise, Leakage power, Multi-threshold CMOS, Full adder, Pass transistor logic, Sleep transistor, Arithmetic Operation.

I. INTRODUCTION

The adders are heart of complex arithmetic's and computational circuits such as multiplier, compressor large adder, comparator and parity checkers [1],[2],[3]. Thus, enhancing the performance of the full adder block leads to the enhancement of the overall system performance. In recent years, various logic approaches have been proposed to implement low power adder. Most of the VLSI applications, such as video processing, and microprocessors widely use arithmetic operations. Several works have been done in order to decrease transistor count and consequently decrease power consumption and area. Minimizing power dissipation is therefore important, both for increasing levels of integration and to improve reliability, feasibility, and cost. The aim of paper is to implement the full adder to reduce power and increase in speed [4],[5]. For the application of electronic devices, designers have many objects to work within very low leakage power and to meet specification of product battery life and package cost. This paper here aims at design, analysis and improvement of power efficiency and ground bounce noise reduction of the 14T adder at 180nm technology. Here, we have as to summarize some performances criteria and optimization of the adder cells for active power, leakage power and ground bounce noise with respect to various voltage and temperatures. In this paper, we have proposed to devolved design techniques with 14T adder to reduce static power dissipation and reduce ground bounce noise. The power reduction in any logic circuit cannot be achieved with trading off performance because it can make harder to reduce to leakage during run time operation [6]. We have seen several techniques proposed to reduce leakage power [7]. The paper here describes proposed stacking power technique where sleep transistor is added between active ground rail and virtual ground [10].The main idea behind this technique is to turnoff device in sleep mode and cut off leakage path provides a reduced leakage with improved power performance [11][12] and reduction in ground bounce noise with proposed novel technique with improved stacking and power gating.

II. THE 14T FULL ADDER

The increasing demand for portable equipments such as cellular phones, personal digital assistant (PDA), and notebook personal computer, arises the need of using area and power efficient VLSI circuits. Full adder has been derived with various structures previously to reduce the power dissipation and area reduction [16]. To analyze different parameters of the adders we use the 14T full adder as our base structure. The structure shown in Fig1., uses pass transistor logic for leakage and area reduction [5]. However still having

less number of transistors and reduced leakage, the 14T adder suffers from ground bounce noise.

$$SUM=((A\oplus B)\oplus Cin) \quad (1)$$
$$Cout=AB+(A\oplus B)Cin \quad (2)$$

TABLE I. Truth Table 14T Full Adder

A	B	Cin	Cout	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

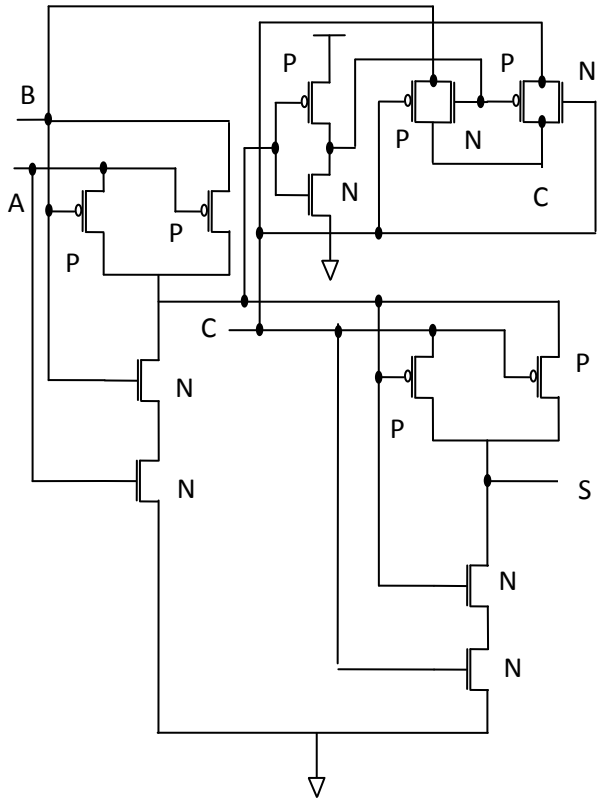


Fig.1. Schematic of 14T Full Adder

III. MTCMOS TECHNIQUE

In MTCMOS technique, transistors of low threshold voltage become disconnected from power supply by using high threshold sleep transistor on the top and bottom of the logic circuit. The multi threshold CMOS technology has two main features. This technique based on disconnecting the low threshold voltage (low-Vt) logic gates from the power supply and the ground line via cut-off high threshold voltage (high-Vt) sleep transistors is also known as "power gating".

The ground bounce noise does not affect the circuit operating at lower clock frequencies. At higher frequencies the switching due to ground bounce noise will change the state of actual output[10] . The reduce ground bounce noise 14T adder shows in Fig. (2) and Fig. (3).

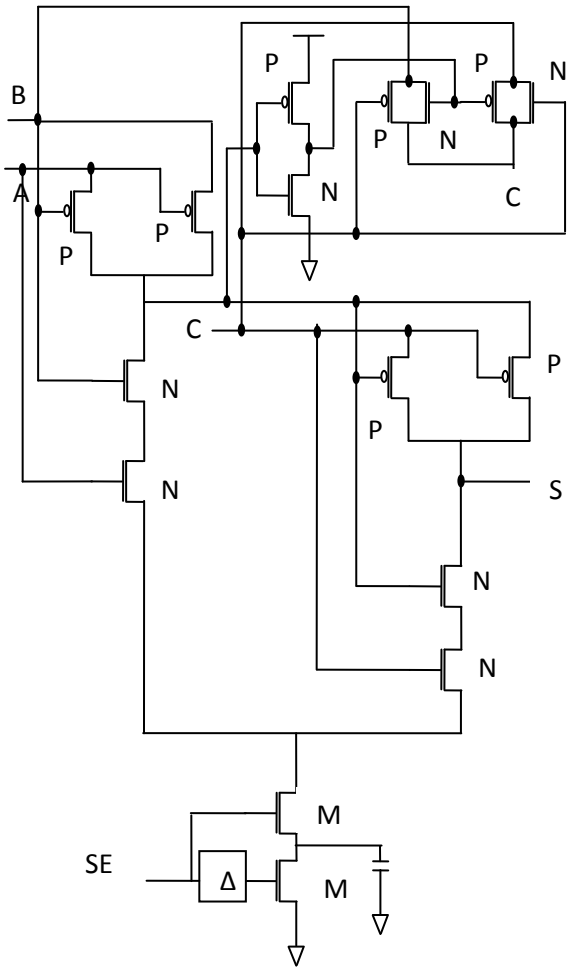


Fig .2. 14T Full Adder with sleep transistor

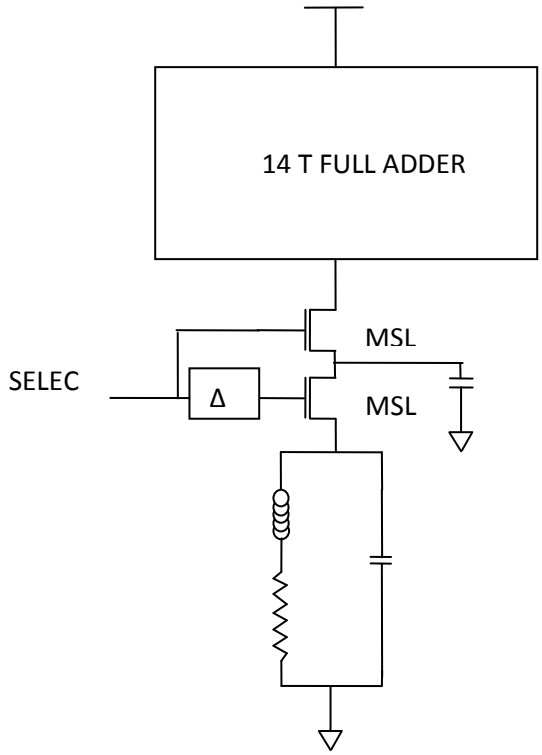


Fig.3 14 T Full Adder with stacking power gating

To decrease the ground bounce noise and leakage power, so we will proposed a modified design with the stacking power gating technique in Fig. (3) and (4). In this technique stack sleep transistor is connected to the virtual ground of the circuits to reduce the magnitude of voltage glitches and current and reduction of leakage power by stacking effect, when both the sleep transistor ST1 and ST2 is turn off (sleep mode). Here with help of select input we have reduced ground bounce noise and this is achieved by the adjusting both the transistor with help of ΔT (delay between the both sleep transistor) (sleep to active mode) [10].

IV. PERFORMANCE ANALYSIS AND SIMULATION RESULT

In this section, we have performed simulation of our conventional 14T and modified 14T adder (adder with stacking) on Empyrean Aether Tool at 180nm Technology.

A. ACTIVE POWER

At the time of operating the power is dissipated by the circuit is known as active power. Active power includes both static power and dynamic power of the circuit. Here we will calculate the active power of the circuit at basic of voltage and temperature for the 180nm technology. The Active power consumption of CMOS circuit [8][9] is consumed by the following equation:

$$P_{active} = P_{dynamic} + P_{static} \quad (3)$$

$$P_{avg} = P_{switching} + P_{short\text{-}circuit} + P_{leakage} \quad (4)$$

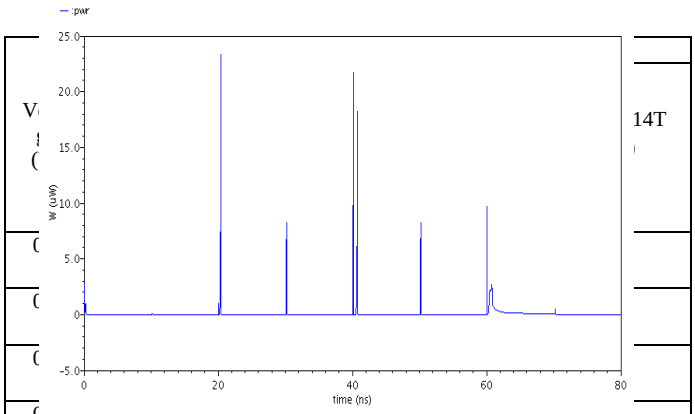
$$P = (\alpha_{0->1} C_L \cdot V^2_{dd} \cdot f_{clk}) + (I_{sc} \cdot V_{dd}) + (I_{leakage} \cdot V_{dd}) \quad (5)$$

The first term represents the switching component of power, where C_L is the load capacitance, f_{clk} is the clock frequency and $\alpha_{0->1}$is the probability that a power consuming transition occurs (the activity factor).The second term is due to the direct-path short circuit current, I_{sc}, which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current, $I_{leakage}$. As shown the table 1 in the case of modified 14T adder with stacking power gating active power is reduced compared to conventional 14T adder .the reduction almost 54.39 % at voltage 0.7 V and temperature 27^o C.

TABLE II
ACTIVE POWER DISSIPATION OF 14T ADDER

Circuit	Conventional 14T Adder (μW)		Modified 14T Adder (μW)	
Active power	0.7 V	27^o C	0.7 V	27 ^{o}C
	78.21	78.21	42.54	42.54

Avg. 78.21



1.0	52.68	453.7	127.2	110.4

Fig.5 (a) Active power wave of conv. 14T

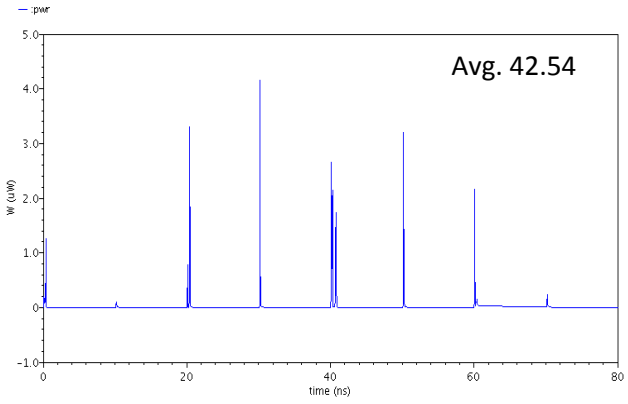


Fig. 5(b) Active power wave of modified 14T

B. STAND BY LEAKAGE CURRENT

The stand by leakage is obtained when the circuit in idle mode. Here we connect the sleep transistor to the pull down network of 14T adder circuit and ground of the circuit. When we measuring the leakage current in stacking power gating then both transistor is off [10] .The basic equation of stand by leakage is [14]

$$I_{leak} = I_{sub} + I_{ox} \qquad (6)$$

Where, I_{sub} = Sub threshold leakage current,

I_{ox} = Gate oxide current.

Stand by leakage current is measured by at 0.7V and 27^{o}C. It is greatly reduced almost 80 % in modified 14T adder with stacking power gating. The table II shows the leakage current at various voltages and various temperatures.

TABLE III
THE STAND BY LEAKAGE CURRENT AND POWER
TABLE (A)

TABLE (B)

Temp. ^{0}C	Leakage current		Leakage power	
	Conv. 14T (nA)	Modified 14T(fA)	Conv. 14T (uW)	Modified 14T (uW)
27	32.19	414.1	17.31	11.83
47	32.42	814.7	18.07	57.15
67	32.53	1020.3	19.02	68.44
87	32.77	1423.6	22.12	79.53
107	32.96	2023.5	28.43	83.23

C. LEAKAGE POWER

The stand by leakage power is measured at the time of idle mode. Here measured the leakage power when the sleep transistor is off. Basically the stand by leakage power is the product of the leakage current and supply voltage [13]. The basic equation of leakage power is

$$P_{leak} = I_{leak}.V_{dd} \qquad (7)$$

The table (A) and Table (B) shows leakage power is reduced in various voltages and temperatures after applying stacking power gating.

D. GROUND BOUNCE NOISE

During the active mode of the circuit an instant current pass from sleep transistor, which is saturation region and causes a sudden rush of the current. Elsewhere , because of self inductance of the off- chip bonding wires and parasitic inductance on chip power rails , result voltage function in the circuit depends on input / output buffers and internal circuitry . The noise depends on the voltage. The ground bounce noise mode is in Fig (5).[14][15].

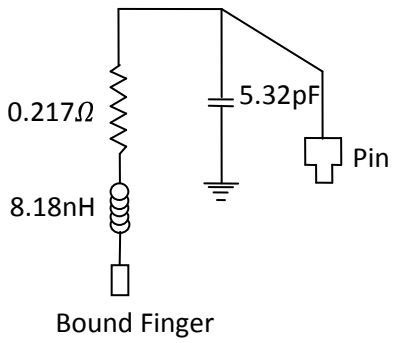


Fig. 6. DIP-40 package pin ground bounce noise mode

TABLE IV
GROUND BOUNCE NOISE FOR 14T ADDER

Voltage (V)	Ground Bounce Noise (uV)		Temp. (^{0}C)	Ground Bounce Noise (uV)	
	Conventional	Modified		Conventional	Modified
0.4	2.44	0.01	27	10.5	0.31
0.5	4.23	0.07	47	13.2	0.49
0.6	8.14	0.24	67	14.4	0.44
0.7	10.5	0.31	87	16.8	0.62
1	18.6	1.86	107	26.5	0.59

As shown in the table, the ground bounce noise is reduced up to 90 % in to various voltage and temperature.

V. CONCLUSION

In this paper we proposed a modified pass transistor based14T Adder for microprocessor and arithmetic logic circuit with low ground bounce noise and reduced standby leakage current and leakage power. Here we have used high performance power gating technique (FBB Multimode MTCMOS) to reduced active power, leakage power, standby leakage current and ground bounce noise. The leakage current up to 80% and leakage power up to 70 %. The ground bounce noise is reduced to up to 90 % and active power is reduced up to 54.39 %. The proposed modified 14T adder is operated at various voltages and various temperatures.

ACKNOWLEDEMENT

This work is supported by Rama University Uttar Pradesh, Kanpur.

REFERENCES

[1] Radu Zlatanovici, Sean Kao, Borivoje Nikolic, "Energy-Delay of Optimization 64-Bit Carry- Lookahead Adders With a 240ps 90nm CMOS Design Example," *IEEE J. Solid State circuits*, vol.44, no. 2, pp. 569-583, Feb. 2009.

[2] K.Navi, O. Kavehei, M. Rouholamini, A. Sahafi, S. Mehrabi, N. Dadkhai, "Low-Power and High-Performance 1-bit CMOS Full Adder Cell," *Journal of Computers*, Academy Press, vol. 3, no. 2, Feb. 2008.

[3] Tripti Sharma, K.G.Sharma, Prof.B.P.Singh, "High Performance Full Adder Cell:Comparative Analysis", Proceedings of 2010 IEEE Students' Technology Symposium, IIT Kharagpur, 3-4 April 2010.

[4] Harmander Singh, Kanak Agarwal, Dennis Sylvester, Kevin J. Nowka,"Enhanced Leakage Reduction Techniques Using Intermediate Strength Power Gating,"*IEETransactions on VLSI Systems*,Vol.15, No.11, November2007.

[5] Tripti Sharma, Prof.B.P.Singh, K.G.Sharma, Neha Arora Electronics & Communication Deptt. MITS Deemed University, Rajasthan INDIA, "High Speed, Low Power 8T Full Adder Cell with 45% Improvement in Threshold Loss Problem", Recent Advances in Networking, VLSI and Signal Processing.

[6] Mohammad Hossein Moaiyeri and Reza Faghih Mirzaee, Keivan Navi, "Two New Low-Power and High-Performance Full Adders", Journal Of Computers, Vol. 4, No. 2, February 2009.

[7] T. Vigneswaran, B. Mukundhan, and P. Subbarami Reddy, "A Novel Low Power, HighSpeed 14 Transistor CMOS Full Adder Cell with 50% Improvement in Threshold Loss Problem", World Academy of Science, Engineering and Technology 13, 2008.

[8] R. Bhanuprakash, Manisha Pattanaik and S. S. Rajput, " Analysis and Reduction of Ground Bounce Noise and Leakage Current During Mode Transition of Stacking Power Gating Logic Circuits ",IEEE Region 10 Conference TENCON 2009, pp. 1-6.

[9] Charbel J. Akl, Rafic A. Ayoubi, Magdy A. Bayoumi, "An effective staggered-phase damping technique for suppressing power-gating resonance noise during mode transition," *10th International Symposium on Quality of Electronic Design*, pp.116-119, 2009.

[10] Neil H. E. Weste, David Harris and Ayan Banerjee, "CMOS VLSI Design: A Circuit and System Perspective", Pearson Education, Third Edition 2011.

[11] Manisha Pattanaik, Muddala V. D. L. Varaprasad and Fazal Rahim Khan " Ground Bounce Noise Reduction of Low Leakage 1-bit Nano-CMOS based Full Adder Cells for Mobile Applications", International Conference on Electronic Devices, Systems and Applications (ICEDSA) 2010, pp. 31-36.

[12] Ku He, Rong Luo, Yu Wang, "A Power Gating Scheme for Ground Bounce Reduction During Mode Transition", 25th International Conference on Computer Design (ICCD) 2007, pp. 388-394.

[13] Yingtao Jiang, Abdulkarim Al-Sheraidah, Yuke Wang, Edwin Sha and Jin-Gung Chung, "Low Power Full Adder Using 8T Structure", IEEE Transactions on Circuits and Systems – II: Express Briefs, Vol.51, No.7, July 2004.

[14] Nirmal U.,Sharma G.,Mishra Y., "Low Power Full Adder Using MTCMOS Technique" in proceeding of International Conference

on A d v a n c e s i n I n f o r m a t i o n , Communication Technology and VLSI Design, Coimbatore, India, August 2010.

[15] Adarsh Kumar Agrawal, Shivshankar Mishra, and R. K. Nagaria, "Proposing a Novel Low-Power High-Speed Mixed GDI Full Adder Topology", accepted in Proceeding of IEEE International Conference on Power, Control and Embedded System (ICPCES), Dec. 2010.

[16] Suhwan Kim, Chang Jun Choi, Deog-Kyoon Jeong, Stephen V.Kosonocky, Sung Bae Park, Reducing Ground-Bounce Noise and Stabilizing the Data-Retention Voltage of Power Gating Structures, IEEE transactions on Electron Devices, Vol.55, No.1, January2008.

[17] Hemantha S, Dhawan A and Kar H, "Multi-threshold CMOS Design for Low Power Digital Circuits", TENCON 2008-2008 IEEE Region 10 Conference, pp.1-5, 2008.

[18] Nirmal U., Sharma G., Mishra Y.," MTCMOS technique to minimize stand-by leakage power in nanoscale CMOS VLSI", in proceeding of International Conference on System Dynamics and Control, Manipal, India, August 2010.

[19] Nirmal U.,Sharma G.,Mishra Y., "Low Power Full Adder Using MTCMOS Technique"in proceeding of International Conference on Advances in Information, Communication Technology and VLSI Design, Coimbatore, India, August 2010.

[20] Nirmal U.,Sharma G.,Mishra Y.," MTCMOS technique to minimize stand-by leakage power in nanoscale CMOS VLSI",in proceeding of International Conference on System Dynamics and Control,Manipal, India, August 2010.