Analysis and Comprehensive study of Junction-less transistor

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Abstract: Transistors are the fundamental building blocks of modern electronic devices and all existing transistors contain semiconductor junctions. Junction-less transistor is a uniformly doped nanowire without junctions with a wrap-around gate, As the distance between junction in modern device drop below 10nm extraordinarily high concentration gradients become necessary, junction could help chipmakers continue to make smaller device, Here in this paper presented a junction-less transistor in which there are no doping concentration gradient and there are no junction. They have near-ideal sub threshold slope, low leakage currents, and less mobility with gate voltage and temperature than classic Transistors.

General Terms:-Structure and Operating modes of junction-less transistor, Process of Fabrication techniques, comparison between conventional MOSFET and Junction-less transistor.

Keywords:--Junction-less transistor, Gated resistor, silicon nanowire FET, multiple Gate resistors, E-beam lithography

I. INTRODUCTION

The transistor principle was field in Canada by Austrain-Hungarian physicist Julius Edgar Lilienfield continuous devices miniaturization, Transistors are the fundamental building blocks of modern electronic devices and all existing transistors contain semiconductor junctions. The most common type of junction is the p–n junction, which is formed by the contact between a p-type piece of silicon doped with impurities to create an excess of holes and an n-type piece of silicon, doped to create an excess of electrons. Other junctions include the hetero-junction, it can either be a P-N junction or an N-N (p-p) junction. When the two semiconductor have the same type of conductivity such as P-P,(N-N)the junction is called as isotype hetero-junction, The bipolar junction transistor contains two p–n junctions, and so does the MOSFET (metal-oxide–semiconductor field-effect transistor).The JFE (junction field-effect transistor) has only one p–n junction and the MESFET (metal– semiconductor field-effect transistor) contains a Schottky-junction.

II. MOOR'S LAW

According to moor's law transistors has been doubled every year. So this law is known as the limit for the number of transistors on the most complex chips. Recent trends show that this rate has been maintained into 2015. The law became something of a self-fulfilling prophecy as microchip and electronics manufacturers competed to develop faster, smaller, and cheaper electronic devices; by the early 21st cent., the number of transistors on a typical memory chip had gone far beyond 1 billion. It is generally accepted that technological improvements in miniaturization and microelectronics reach a point where circuits are only a few atoms wide, making it physically impossible to make them even smaller. Transistors are becoming so tiny that it is becoming increasingly difficult to create high-quality junctions. In particular, it is very difficult to change the doping concentration of a material over

distances shorter than about 10 nm. Junction-less transistors could therefore help chipmakers continue to make smaller and smaller devices.

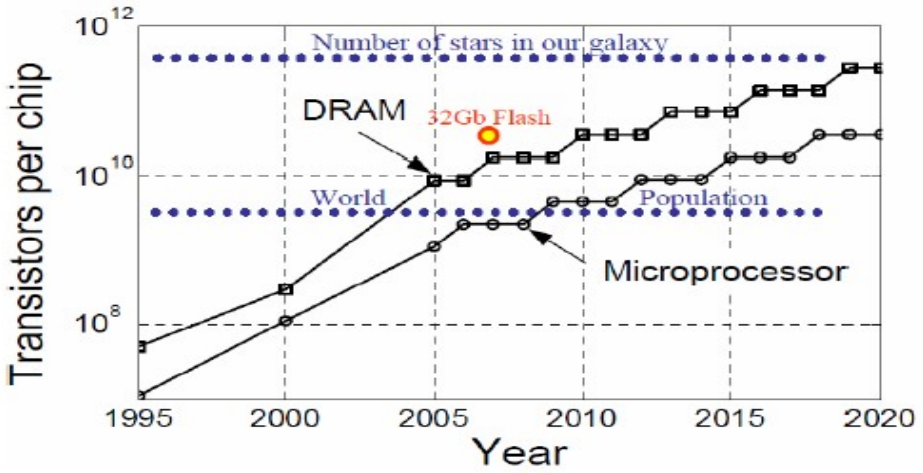


Fig1. Moor's law of evolution

III. STRUCTURE OF JUNCTIONLESS TRANSISTOR

The invention transistor- and diode-action has depended on controlling the flow of electrons across junctions giving rise to the familiar NPN and PNP notation for bipolar devices and p- and n-type FETs with sources and drains. Controlling the junction allows the current in the device to be turned on and off and it is the precise fabrication of this junction that determines the characteristics and quality of the transistor and is a major factor in the cost of production. However, as consequence of the repeated miniaturization predicted by Moore's Law transistors at the leading edge are becoming so small that conventional transistor architectures are becoming exceedingly difficult to fabricate

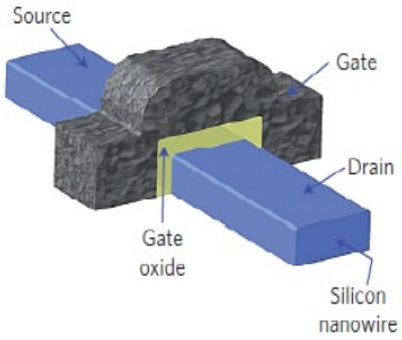


Fig2. Schematic of an n-channel nano-wire transistor

The Lilien-field transistor is a field-effect device, much like modern metal-oxide–semiconductor (MOS) devices. It consists of a thin semiconductor film deposited on a thin insulator layer, itself deposited on a metal electrode. The latter metal electrode serves as the gate of the device. In operation, the current flows in the resistor between two contact electrodes, in much the same way that drain current flows between the source and drain in a modern MOSFET. The Lilien-field device is a simple resistor, and the application of a gate voltage allows the semiconductor film of carriers to be depleted, thereby modulating its conductivity. Ideally, it should be possible to completely deplete the semiconductor film of carriers, in which case the resistance of the device becomes quasi-infinite. The Lilienfield transistor, unlike all other types of transistors, does not contain any junction. A transistor is a solid-state active device that controls current flow, and the word 'transistor' is a contraction of transistor. The Lilienfield transistor is a gated trans-resistor; that is, it is a resistor with a gate that controls the carrier density, and

hence the current flow. It is the simplest and first patented transistor structure; Lily-field's transistor would never have been able to produce a working device.

Fig 2 presents a schematic view of a junction-less nano-wire gated resistor. Having no junctions presents a great advantage. Modern transistors have reached such small dimensions that ultra-sharp doping concentration gradients are required in junctions: typically the doping must switch from n-type with a concentration of 1× 1019 cm-3 to p-type with a concentration of 1× 1018 cm-3 within a couple of nano-metres,This imposes severe limitations on the processing thermal budget and necessitates the development of costly millisecond annealing techniques. In a junction-less gated resistor, on the other hand, the doping concentration in the channel is identical to that in the source and drain. Because the gradient of the doping concentration between source and channel or drain and channel is zero, no diffusion can take place, which eliminates the need for costly ultrafast annealing techniques and allows one to fabricate devices with shorter channels. The key to fabricating a junction-less gated resistor is the formation of a semiconductor layer that is thin and narrow enough to allow for full depletion of carriers when the device is turned off. The semiconductor also needs to be heavily doped to allow for a reasonable amount of current flow when the device is turned on. Putting these two constraints together imposes the use of Nano scale dimensions and high doping concentrations. The operation principle of the gated resistor has recently been investigated through simulations by several research groups.

IV Operating Modes:-

The channel region in a gated resistor is neutral in the centre of the nanowire and because the carrier are located in neutral silicon, they see a zero electric field in the directions perpendicular to the current flow. When the device is fully turned on, assuming a low drain voltage for simplicity, the entire channel region is neutral and in flatband conditions. The channel then effectively behaves as a resistor with conductivity $\sigma = q\mu ND$, and the mobility is that of carriers traveling through bulk silicon. The mobility of electrons in heavily doped n-type silicon is ~110 $cm^2 V^{-1} s^{-1}$; it varies very little for doping concentrations ranging from 1x1010 to 1x1015 cm^{-3}. In a similar way, hole mobility hovers around 35$cm^2 V^{-1} s^{-1}$ in p-type silicon for the same doping 15concentrations. These mobility values may seem rather low, but they are to be placed in the context of modern short-channel MOSFETs. In unstrained silicon, the effective channel mobility of bulk MOSFETs drops from 350 $cm^2 V^{-1} s^{-1}$ at the 0.8 μm node to 100 $cm^2 V^{-1} s^{-1}$ at the 0.13 μm node. Similarly, a drop of peak mobility from 300 to 140 $cm^2 V^{-1} s^{-1}$ is reported in Fin FETs when the gate length is reduced from 0.9 to 0.11 μm. If it was not for straining techniques, the electron mobility at the 45 nm node would be well below 110 $cm^2 V^{-1} s^{-1}$. These straining techniques can, of course, be applied to gated resistors as well inversion-mode transistors. In a MOSFET, carriers are confined in an inversion channel in which scattering events rapidly increase in frequency with gate voltage, thereby decreasing transconductance and current drive. In the heavily doped gated resistor, the drain current essentially flows through the entire section of the nanoribbon, instead of being confined in a surface channel. Figure 2 shows the electron concentration in an n-type junctionless gated resistor for different values of gate voltage ranging from device pinch-off to flatband conditions . The conduction path is clearly located near the centre of the nanowire, and not at the silicon–SiO2 interfaces. This allows for the electrons to move through the silicon with bulk mobility, which is influenced much less by scattering than the surface mobility experienced by regular transistors. It is, however, possible to create surface accumulation channels by increasing the gate voltage beyond the flatband voltage, if a resistor sees its transconductance degrade much more slowly when gate voltage is increased. As a result, higher current and, therefore, higher-speed performance, can be expected from the gated resistor. The variation of the threshold voltage of a gated resistor with temperature is similar to that of a bulk MOSFET, with values of approximately -1.5 mV^oC^{-1} measured in our devices. Interestingly, the decrease of mobility with temperature is much smaller in the gated resistors than in tri-gate FETs. In a lightly doped FET, the mobility is little affected by impurity scattering and tends to be phonon limited, so it shows a strong temperature dependence. In the highly doped gated resistor, on the other hand, mobility is limited by impurity scattering rather by phonon scattering, and its variation with temperature is much smaller. For instance, the electron mobility measured at room temperature in trigate FETs and gated resistors are 300 and 100 $cm^2 V^{-1} s^{-1}$, respectively. When heated to 200ºC, the trigate FETs show a 36% loss of mobility, whereas the gated resistor has a reduction in mobility of only 5%.further increase of drain current is desired. Because it operates under bulk conduction rather than channel conduction, the gated resistor sees its trans-conductance degrade much more slowly when gate voltage is increased. As a result, higher current and, therefore, higher-speed performance,

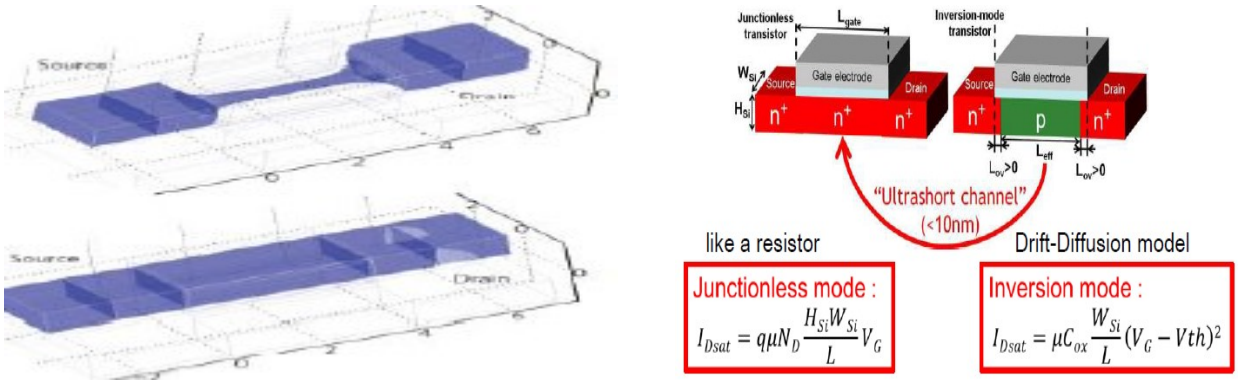


Fig2:- Operating modes of junctionless transistor

V. PROCESS OF FABRICATION TECHNIQUES

The key to fabricating a junctionless gated resistor is the formation of a semiconductor layer that is thin and narrow enough to allow for full depletion of carriers when the device is turned off. The semiconductor also needs to be heavily doped to allow for a reasonable amount of current flow when the device is turned on. Putting these two constraints together imposes the use of nanoscale dimensions and high doping concentrations.The junction-less nanowire transistor (JNT) is a heavily doped SOI nano-wire resistor with an MOS gate that controls current flow. Doping concentration is constant and uniform throughout the device and typically ranges from 1010 and 1015 cm^{-3}. The device features bulk conduction instead of surface channel conduction. Junction-less fabrication process is greatly simplified, compared to standard CMOS since there are no doping concentration gradients in the device. Structure with poly-silicon gate is shown in

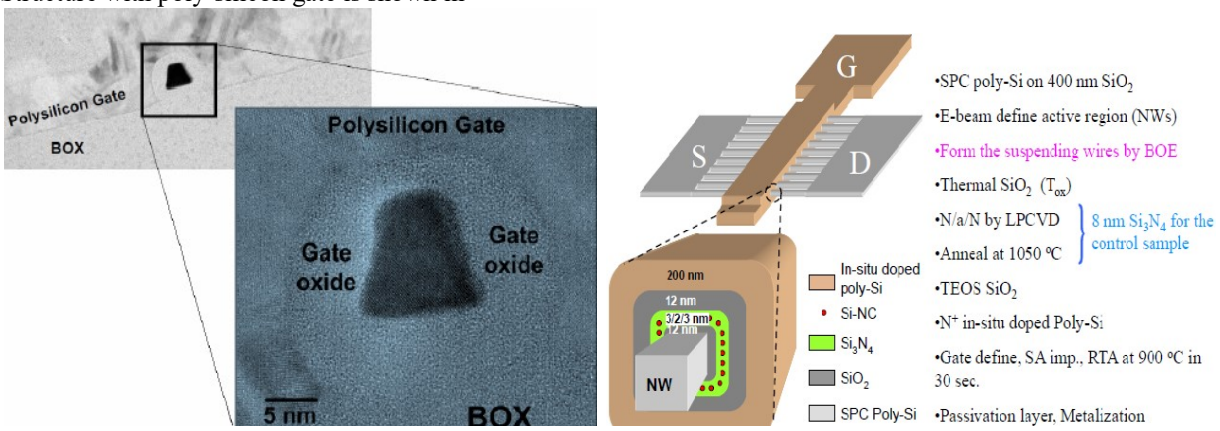


Fig3. Cross sectional TEM picture of transistor showing the structure of the device.

Junction-less nano-wire transistors with gate length down to 40 nm were fabricated using the process described. The gate oxide thickness is 5 nm and beam lithography was used to pattern both the nanowires and the gates. The n-channel devices were doped using arsenic to a channel concentration of 5x1010cm^{-3} and P+ poly-silicon was used as gate material.

VI. SHORT CHANNEL EFFECTS

Short-channel effects are predicted to be less important in junctionless devices it is shown that drain-induced barrier lowering (defined measuring the reduction of the energy barrier when it is applied the same VD used to define the I current) is lower than in equivalent inversion-mode devices, especially for the shortest devices. In MOSFET with junctions, part of the reduction of the threshold short-channel effects is due to the presence of a space-charge region associated with the junctions (SCE in equation below), and part of it (DIBL) is due to the growth of the drain space-charge region with drainvoltage:

$$Vth = V_{tho}\text{-SCE-DIBL}$$

Where V_{tho} is the long-channel threshold voltage .In a MOSFET with physical gate length $L_{physical}$ the effective gate length is Leff when the device is on, and the effective gate length is LSCE when the device is off. Note that LSCE<L_{eff}, which means that the "effective" channel length when the device is off is shorter than when it is on. In the junctionless transistor, the doping concentration is constant across the device. The electrostatic squeezing" of the

channel in the off device propagates into the source and drain; as a result, $L_{eff}>L_{physical}$ when the device is off. When the device is on, the "squeezing" effect is removed, such that $L_{eff}=L_{physical}$ As a result, L_{eff} larger on the off state than in the on state, which improves short-channel effects.

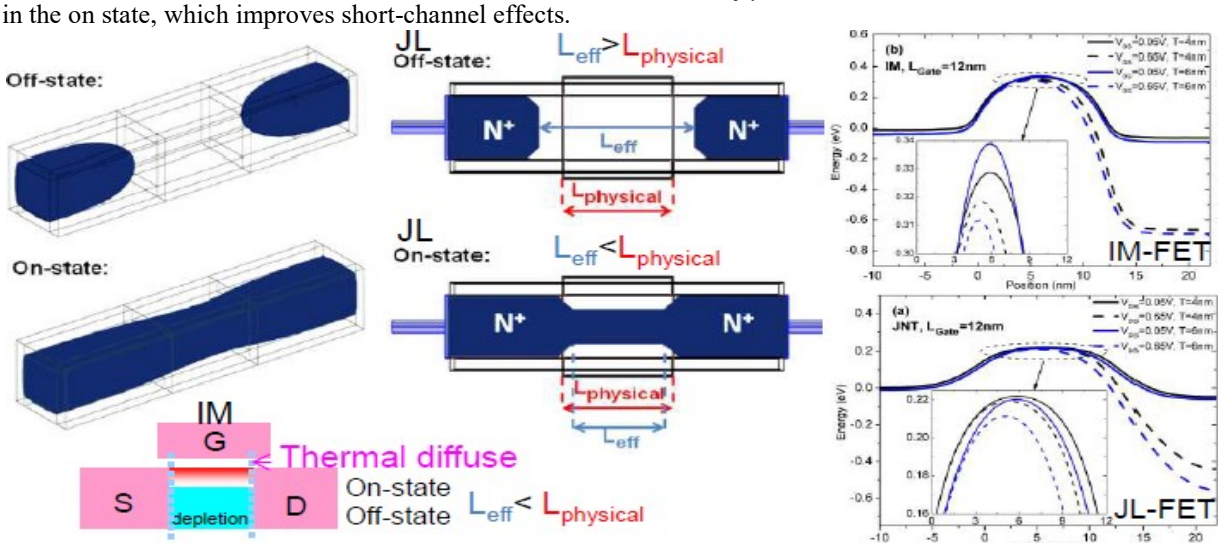


Fig :- short channel effects in transistor

VII. LEAKAGE CURRENT

According to Monte Carlo Fig. 4 shows the results for the leakage current (*I* off), defined for the same drain voltage but without applying the gate voltage required to decrease the energy barrier created by the work function difference between gate and channel

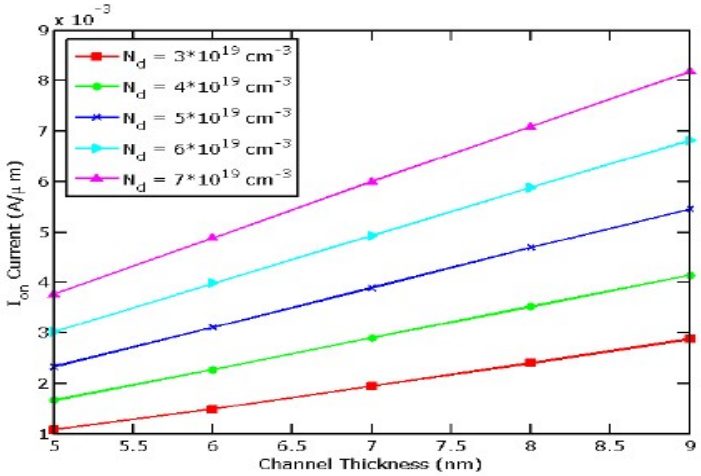


Fig4. *I*on current in function of channel thickness and doping

concentration. *L*G = 15 nm; *V*G = *V*D = 1.0 V. Controlling the Gate like a wedding ring: "The current flows in a very thin silicon wire and the flow of current are perfectly controlled by a "wedding ring" structure that electrically squeezes the silicon wire in the same way that you might stop the flow of water in a hose by squeezing it. These structures are easy to fabricate even on a miniature scale which leads to the major breakthrough in potential cost reduction."

VIII. COMPARISON WITH JUNCTION TRANSISTOR

The electric field perpendicular to the current flow is found to be significantly lower in junction-less transistors than in regular inversion-mode or accumulation-mode field-effect transistors. Since inversion channel mobility in metal oxide semiconductor transistors is reduced by this electric field, the low field in junction-less transistor may give them an advantage in terms of current drive for manometer-scale complementary metal-oxide semiconductor applications. This observation still applies when quantum confinement is present. The major carriers in channel region for a Junction transistor make itself a barrier to carrier scattering, whereas, the Junction-less transistor does

not have this problem, leading to get a high current drive. The advantage related to the JL transistors is simple device fabrication due to the elimination of junction implantation and annealing; hence, a simple process results in a reduced cost. These advantages are difficult to be achieved for junction transistors. That is why excluding the so-called short-channel effects (SCEs) the conventional CMOS devices face lots of critical issues for achieving low-cost mass production. Fig 5 shows electric field of with junction and without junction transistor.

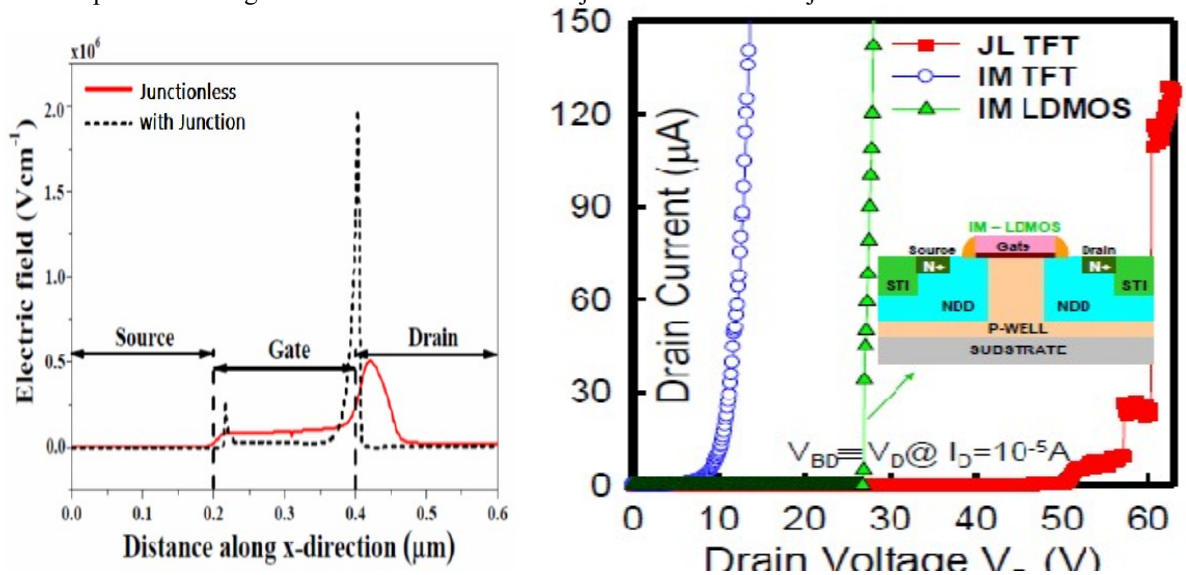


Fig 5. Electric field of with junction and without junction transistor.

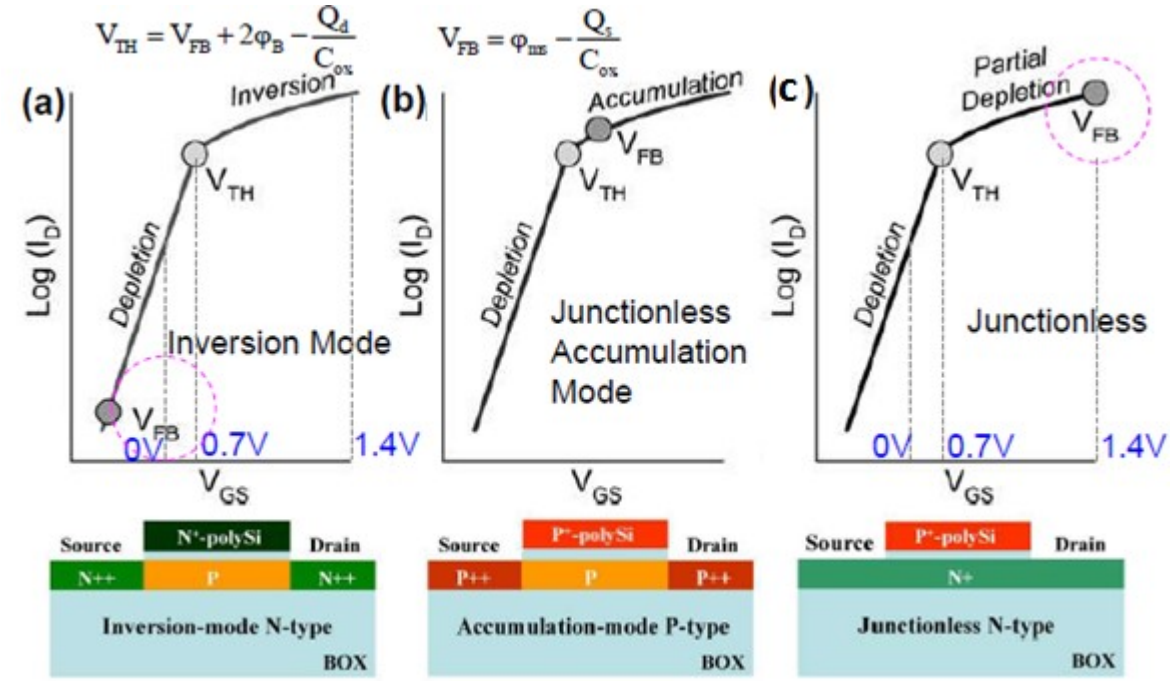
Both devices are biased in the sub threshold regime with *VDS*=1V and *VG*=*VTH*-200mV. As expected the peak electric field of the inversion-mode device is at the drain junction and the drain electric field extends to some distance in the channel region, contributing to both increasing DIBL and reducing the output impedance. In the junction-less device the region of high electric field is in the drain, outside of the region covered by the gate. It is wider than in the inversion-mode device, and the peak value is lower. As a result, the influence of the drain electric field on the channel region is much smaller than in the inversion- mode device, resulting in a smaller DIBL.

XI. CONDUCTION MODES

The physics of the JNT is quite different from that of standard mitigate FETs. Depletion of the heavily doped nanowire creates a large electric field perpendicular to current flow below threshold, but above

State	Inversion mode	Accumulation mode	Junctionless
On state	Main current in Surface inversion channels	Surface accumulation channels, Small body current	Surface accumulation channels are unnecessary Lange body current
OFF state	Surface sub threshold current	Body sub threshold current	Body sub threshold current

threshold the field drops to zero. This is the opposite of inversion-mode (IM) or even accumulation mode (AM) devices where the field is highest when the device is turned on. The electron concentration profiles in cross sections of IM, AM and JNT devices are shown in



Current in inversion-mode (a) Inversion -mode (b) accumulation mode (c) junction-less mode

X. TYPES OF JUNCTIONLESS TRANSISTOR

A. Junctionless MuGFET:

This device has no junctions, a simpler fabrication process, less variability and better electrical property than classical inversion mode.

B. Bulk Planar Junction-less Transistor (BPJLT):

The bulk planar junction-less transistor (BPJLT) is highly scalable source–drain junction- free field-effect transistor. It is thus junction-less in the source–channel–drain path but needs a junction in the vertical direction for isolation purposes.

C. **Junctionless Vertical MOSFET (JLVMOS)**

The junctionless VMOS is based on bulk-Si wafer. The vertical channel of a VMOS is defined by the gate spacer thus the fabrication cost can be reduced drastically. The double-gate scheme of a VMOS helps to increase the gate controllability over the channel region.

XI. CONCLUSION

This paper presents the study of junction-less transistor and compared with other transistor. Junction-less can exhibit low leakage currents and excellent short channel behavior at shorter gate lengths. As we know all existing transistors are based on the use of semiconductor junctions formed by introducing doping atoms into the semiconductor material. According to moor's law the junction-less transistor is best to reduce the size of the transistor with excellent behavior Which makes the chip makers work easy. Junction-less fabrication process is greatly simplified, compared to standard CMOS since there are no doping concentration gradients in the device.

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