Analysis of Low Power 6T SRAM Using 45 nm Technology

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***Abstract*-In this paper we designed SRAM to provide an interface with CPU and to substitute DRAMs in systems that require very low power consumption. Low power SRAM design is critical since it takes a large fraction of total power and die area in high performance CPUs. A SRAM cell must come across the necessities for the operation in Nano ranges. The scaling of CMOS technology has important effects on SRAM cell – random fluctuation of electrical characteristics and substantial leakage current. The random variation of electrical possessions causes the SRAM cell to have huge mismatch in transistor threshold voltage. Thus, the static noise margin (Read Margin) and the write margin are degraded dramatically. The SRAM cell inclines to be unsteady and the low power supply operation becomes hard to achieve.**

***Keywords*—SRAM; Cadence; Virtuoso; Noise Margin; 45 nm technology**

I. INTRODUCTION

For nearly 40 years CMOS devices have been scaled down in order to achieve higher speed, performance and lower power consumption. Technology scaling results in a significant increase in leakage current of CMOS devices. Static Random Access Memory (SRAM) continues to be one of the most fundamental and vitally important memory technologies today.

Because they are fast, robust, and easily manufactured in standard logic processes, they are nearly universally found on the same die with microcontrollers and microprocessors. Due to device scaling there are several design challenges for nanometer SRAM design. As the
Integration density of transistors increases; power consumption has become a major concern in todays
processors and SoC designs. Considerable attention has been paid to the design of low power and high-performance
SRAMs as they are critical components in both handheld devices and high performance processors.

The objective of this paper is to investigate the transistor sizing of the 6T SRAM cell for optimum power and delay. A bit line balancing scheme and transmission gate scheme are proposed for high performance operation of SRAM cell. Cadence simulation results confirm that the proposed scheme achieves nearly 40% of power savings compared to other designs.[1]

II. OPTIMAL SIZING FOR 6T SRAM CELL

A. Sizing of 6T SRAM cell

The SRAM cell should be sized as small as possible to achieve high density in memory design. However, issues related to robustness impose a sizing constraint to the conventional SRAM design. Fig. 1 shows the conventional 6T SRAM cell configuration. The transistor ratio between M3 and M6 must be greater than 1.2 to keep a proper noise margin during the read operation. The proposed 6T SRAM cell uses 1v for its operation when compared to 1.8V used by conventional 180 nm SRAM cell. In this paper, we propose transistor of size 45nm whose voltage of operation is less than 1V.

Each bit in SRAM is stored on four transistors that form two cross coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional transistors serve as the access transistors to control the storage cell during the read and write operations. Access to the cell is enabled by the word line (WL in figure) which controls the two access transistors M5 and M6 which, in turn, control whether the cell should be connected to the bit lines: BL and BL bar. They are used to transfer data for both read and write operations.

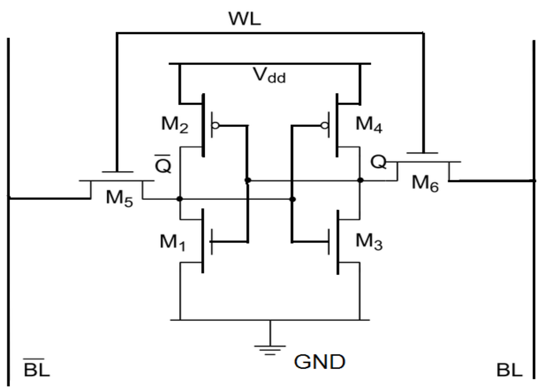

Fig 1: 6T SRAM cell

B. *SRAM Operation*

An SRAM cell has three different states it can be in: standby where the circuit is idle, reading when the data has been requested and writing when updating the contents. The SRAM to operate in read mode and write mode should have "readability" and "write stability" respectively. The three different states work as follows:

1) *Standby:* If the word line is not asserted, the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross coupled inverters formed by M1 – M4 will continue to reinforce each other as long as they are connected to the supply.

2) *Reading:* Assume that the content of the memory is a 1, stored at Q. The read operation is done by using the sense amplifiers that pull the data and produce the output. The row decoders and column decoders are used to select the appropriate cell or cells from which the data is to be read and are given to the sense amplifiers through transmission gate.

3) *Writing:* The start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BL bar to 1 and BL to 0. A 1 is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. Note that the reason this works is that the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters[2-3].

III. DESIGN FLOW

Cadence design Systems is electronic design automation software and engineering Services Company that offers various types of design and verification tasks that include:

1) Virtuoso Platform - Tools for designing full-custom integrated circuits, includes schematic entry, behavioral modeling (Verilog-AMS), circuit simulation, full custom layout, physical verification, extraction and back-annotation. Used mainly for analog, mixed-signal, RF, and standard-cell designs.
2) Encounter Platform - Tools for creation of digital integrated circuits. This includes floor planning, synthesis, test, and place and route. Typically a digital design starts from Verilog net lists.
3) Incisive Platform - Tools for simulation and functional verification of RTL including Verilog, VHDL and System C based models. Includes formal verification, formal equivalence checking, hardware acceleration, and emulation[3].

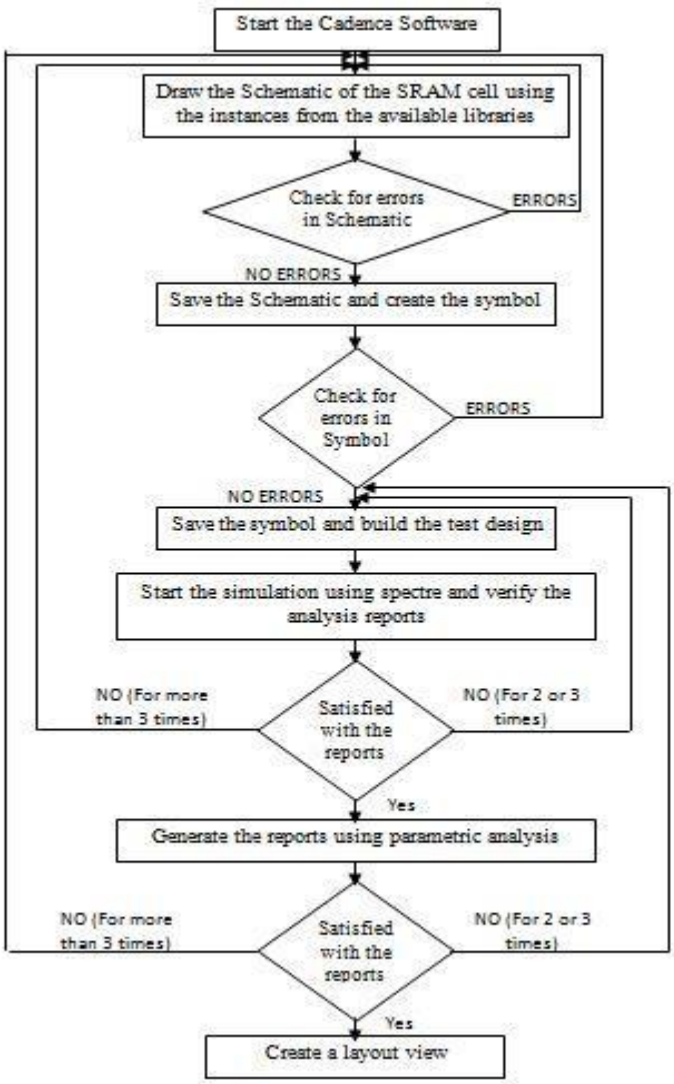

Fig 2: Design Flow

A. *SRAM cell Design*

Single bit storage cell is designed using the nmos and pmos transistors picked from the libraries. The schematic and symbol are as shown below.

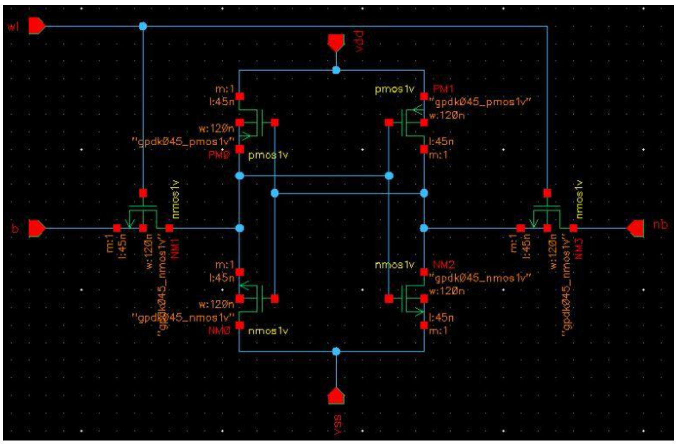

Fig 3: Schematic of SRAM cell

B. Decoder Design

The decoder design depends on the size of the SRAM array that we are going to design. For our simulation, we have used 6to64 decoder. Using this, we can also design larger array in the form of banks. The schematic and symbol are as shown below.

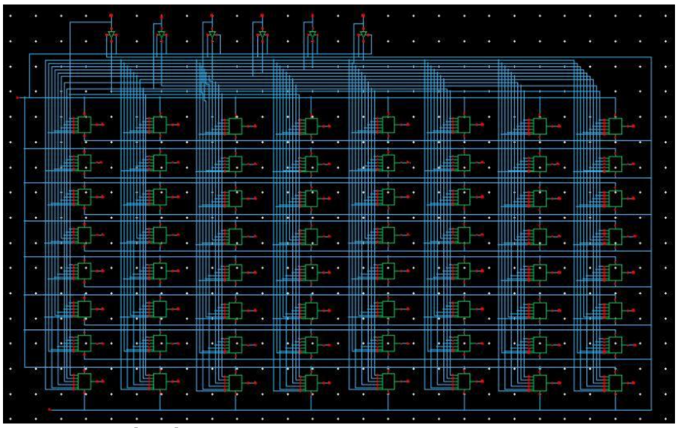

Fig. 4: 6 to 64 decoder

C. Sense Amplifier Design

The sense amplifiers have to amplify the data which is present on the bit lines during the read operation. The memory cells are weak due to their small size, and hence cannot the discharge the bit lines fast enough. Also, the bit lines continue to slew till a large differential voltage is formed between them. This causes significant power dissipation since the bit lines have large capacitances. Hence, by limiting the word line pulse width we can control the amount of charge pulled down by the bit lines and hence limit power dissipation. It consists of two cross coupled gain stages which are enabled by the sense clock signal. The cross coupled stage ensures a full amplification of the input signal. This type of amplifier consumes least amount of power, however they can potentially be slower since some timing margin is needed for the generation of the sense clock signal. If the sense amplifiers enabled before sufficient differential voltage is formed, it could lead to a wrong output. Thus, the timing of the sense clock signal needs to be such that the sense amplifier can operate over various process corners and temperature ranges. The schematic and symbol are as shown below[4-5].

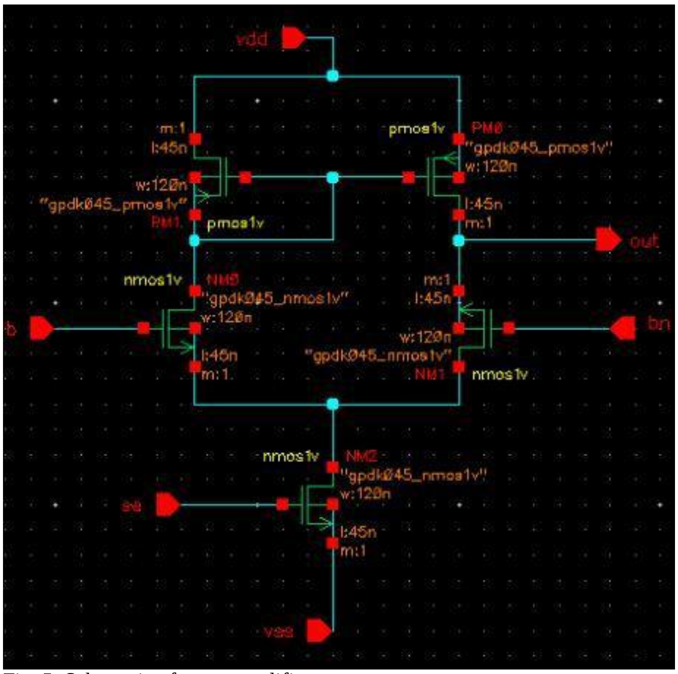

Fig. 5: Schematic of sense amplifier

D. Transmission Gate Design

Transmission gate is used to improve the noise margin. The data, whether from bit or bit bar is given to transmission gate that consists of cascaded nmos and pmos transistors. The input for pmos is 0V, and input for nmos is 1V when the data is to be read from SRAM. The schematic and symbol are as shown below[6].

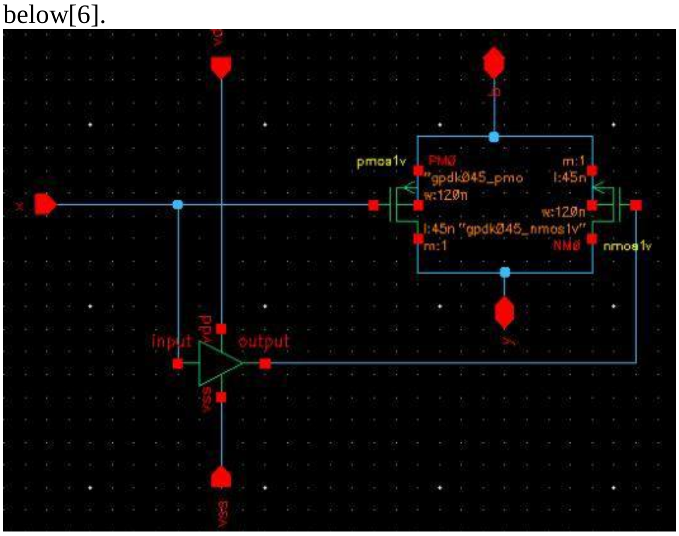

Fig 6: Schematic of Transmission gate

IV. DESIGN OF SRAM ARRAY

The row decoder and column decoder are used to select the particular cell onto which the data is to be written or from which the data is to be read. In our simulation, we designed 64X64 arrays. The schematic of the SRAM array is as shown below[7-9].

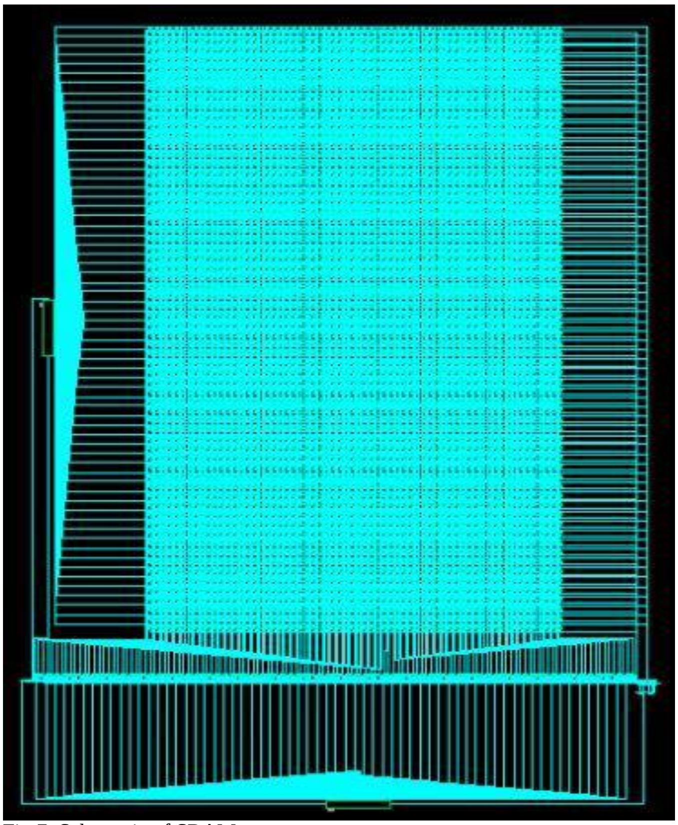

Fig 7: Schematic of SRAM array

V. SIMULATION RESULTS

Cadence simulation of transient analysis and DC analysis gave good results. The results are shown in the timing diagram. The noise margins are very good and the output is stable.

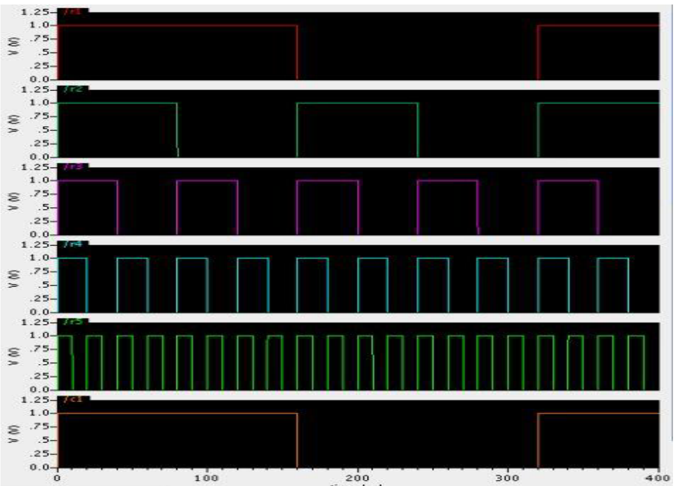

Fig 8: Timing Diagram

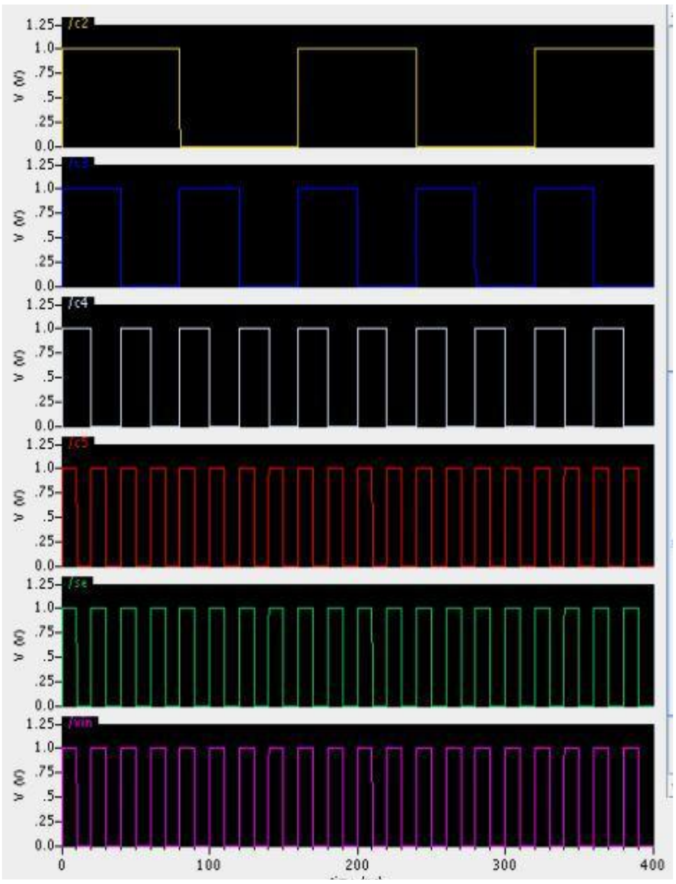

Fig 9: Timing diagram

VI. CONCLUSION

This paper presents the design of SRAM array in 45 nm having very low power consumption. The low power design of SRAM is investigated and 6T SRAM architecture is chosen for memory bit cell and an array is designed with that bit cell. Transient and parametric analyses were carried out in the simulation process and the power consumption is estimated. As stated earlier, the power consumption can further be reduced by partitioning the array and by using DWL scheme.

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