Design and Analysis of Low power Carry Look ahead Adder using forward body biased Stacking Power Gating Technique.

Priyanka Singh
M.Tech Student
Rama University, Kanpur, India
priyankas2492@gmail.com
Raghvendra Singh
Assistant Professor
Rama University, Kanpur, India
raghav.raghvendra7@gmail.com

Abstract: In this paper, we have proposed a modified Carry Look ahead adder using multi-threshold CMOS technique. Here we use forward body biased Stacking Power Gating technique to evaluate standby leakage current, power and ground bounce noise. All the simulation in this paper has been carried out using empyrean anther at 180 nm technologies at various voltage and temperatures. The forward body biased (FBB) Stacking Power Gating technique has been implemented on conventional Carry Look ahead adder circuit with 180 nm technology parameters for simulations. By using this technique the standby leakage current reduction can be improved by 42 % and leakage power to 69 % as compared to base Carry Look ahead adder. Ground bounce noise can be reduced to 58 % as compared to the conventional adder.

Keywords: Ground bounce noise, Leakage power, Multi-threshold CMOS, Full adder, Pass transistor logic, Sleep transistor.

I. INTRODUCTION

One of the most important issues in VLSI design is standby leakage current with continuous down scaling in advanced CMOS technology. The leakage current contributes 35-42% in active power [1] of digital circuit. It affects active power; standby power and performance of digital circuits because leakage strongly depends on process variations, increase in number of transistor and technology scaling[2]. In this paper, we have proposed new Carry Look Ahead Adder Adder with low power and reduce ground bounce noise. [3]. For the application of electronic devices, designers have many objects to work with very low leakage power and to meet specification of product battery life and package cost[4]. The main idea behind this paper aims at design, analysis and improvement of power efficiency and ground bounce noise reduction of the Carry Look Ahead Adder at 180nm technology [5]. In this paper, we have proposed to develop design techniques with Carry Look Ahead Adder to reduce standby power dissipation and reduce ground bounce noise. The power reduction in any logic circuit cannot be achieved with trading off performance because it can make harder to reduce to leakage during run time operation [6].We have seen several techniques proposed to reduce leakage power [7]. One of the most important technique Stacking Power

Gating also known as power gating technique is used for reducing the leakage current and standby leakage power when device is in idle mode and to improve the performance of device in active mode. The main idea behind this technique is to turnoff device in sleep mode and cut off leakage path provides a reduced leakage with improved power performance and reduction in ground bounce noise with proposed novel technique with improved stacking and power gating[8].

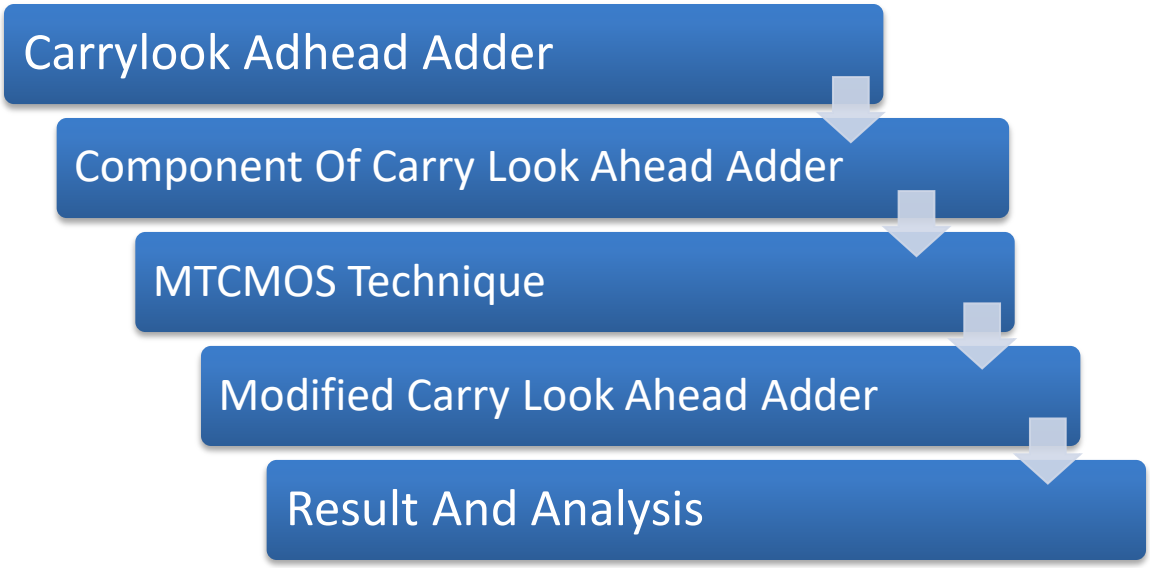

Figure1. Schematic diagram of proposed methodology

II. PROPOSED METHODOLOGY

We have proposed a modified Carry look Ahead Adder based on using forward body biased (FBB) Stacking Power Gating technique CMOS technique .Here we use forward body biased (FBB) Stacking Power Gating technique to evaluate standby leakage current, power and ground bounce noise.

A. Carry Look Ahead Adder:

A Carry Look ahead adder is a fast parallel adder as it reduces the propagation delay by more complex hardware; there are faster ways to add two binary numbers by using carry look ahead adders[7]. They work by creating two signals P and G known to be **Carry Propagator** and **Carry Generator**. The signal from input carry C_{in} to output carry Cout requires an AND gate and an OR gate. Carry Look Ahead Adder Generate two Signals P (Carry Propagator) and other G (Carry Generate) The corresponding Boolean expressions are given here to construct a carry look ahead adder. In the carry-look ahead circuit we need to generate the two signals carry propagator (P) and carry generator (G).

$$Pi = Ai \oplus Bi \dots\dots\dots\dots\dots\dots\dots\dots\dots (1)$$

$$Gi = Ai \cdot Bi \dots\dots\dots\dots\dots\dots\dots\dots\dots (2)$$

The output sum and carry can be expressed as

$$Sum = Pi \oplus Ci \dots\dots\dots\dots\dots\dots\dots\dots (3)$$

$$Ci + 1 = Gi + (Pi \cdot Ci) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4)$$

Having these we could design the circuit. We can now write the Boolean function for the carry output of each stage and substitute for each Ci its value from the previous equations:

$$C1 = G0 + P0 \cdot C0 \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (5)$$

$$C2 = G1 + P1 \cdot C1 = G1 + P1 \cdot G0 + P1 \cdot P0 \cdot C0 \ldots\ldots\ldots\ldots\ldots\ldots\ldots (6)$$

$$C3 = G2 + P2 \cdot C2 = G2P2 \cdot G1 + P2 \cdot P1 \cdot G0 + P2 \cdot P1 \cdot C0 \ldots\ldots\ldots (7)$$

$$C4 = G3 + P3 \cdot C3 = G3P3 \cdot G2P3 \cdot P2 \cdot G1 + P3 \cdot P2 \cdot P1 \cdot G0 + P3 \cdot P2 \cdot P1 \cdot C0 \ldots\ldots\ldots (8)$$

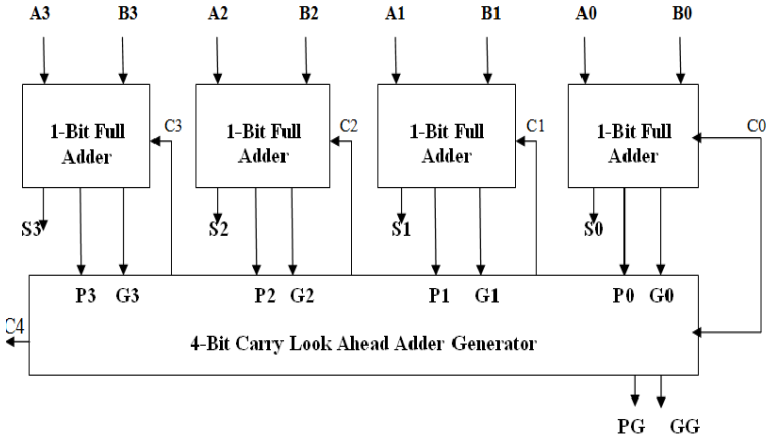

Figure1. Carry Look Ahead Adder

B. COMPONENT OF CARRY LOOK AHEAD ADDER

- **10T FULL ADDER**

We use the pass transistor 10T full adder as our base structure. The structure shown in Fig (1), adopt 3- module implementation, sum, carry and XOR module [13][14]. Here Full Adder uses pass transistor logic for standby leakage and area reduction. However still having less number of transistors and reduced leakage,

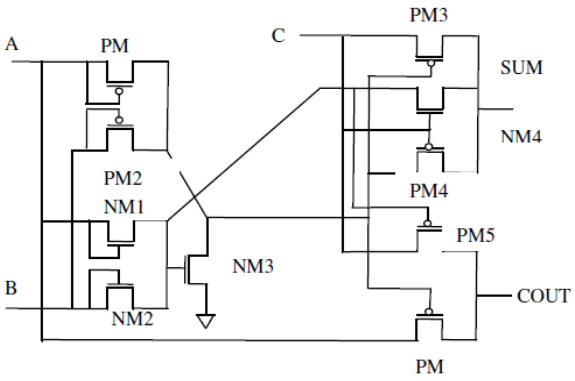

Figure 2. 10 T Full Adder

- **AND GATE:** Conventional AND Gate is the combination of PMOS and NMOS [14]. The circuit shows the realization of CMOS AND gate.

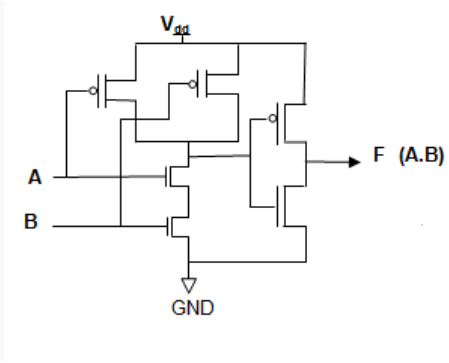

Figure 3 Conventional AND Gate

- **OR GATE:** Conventional OR Gate is the combination of PMOS and NMOS. The circuit shows the realization of CMOS OR gate.

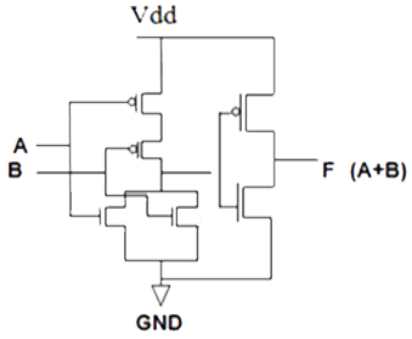

Figure 4 Conventional OR Gate

C. MTCMOS TECHNIQUE

The power gating circuit could work in three different modes:

- Active mode, in which the sleep transistor is on and the circuit function normally.
- Sleep mode, in which the sleep transistor is shut-off and the leakage current of entire circuit is suppressed. The sleep transistor is switched 'off' to block leakage paths between the power and ground rails which could otherwise steadily draw power even during standby.
- Transition mode, in which the sleep transistor is turned on and the circuit goes from sleep to active [15]. Ground Bounce effect usually occurs in transition mode.
- In the active mode, sleep transistors are turned on and the logic consisting of low *VT* transistors can operate with high speed and low switching power dissipation. When the circuit is in sleep mode the high *VT* transistors are turned off cause nag isolation of low *VT* transistor from supply voltage and ground thereby reducing sub-threshold leakage current.

D. MODIFIED CARRY LOOK AHEAD ADDER

A carry-look ahead adder system solves this problem, by computing whether a carry will be generated before it actually computes the sum. There are multiple schemes of doing this, so there is no "one" circuit that constitutes a look-ahead adder [15]. The idea is something like this: To decrease the ground bounce noise and leakage power, so we will proposed a modified design with the stacking power gating technique in Fig. (3) and (4). In this technique stack sleep transistor is connected to the virtual ground of the circuits to reduce the magnitude of voltage glitches and current and reduction of leakage power by stacking effect, when both the sleep transistor ST1 and ST2 is turn off (sleep mode). Here with help of select input we have reduced ground bounce noise and this is achieved by the adjusting both the transistor with help of ΔT (delay between the both sleep transistor) (sleep to active mode) [16]

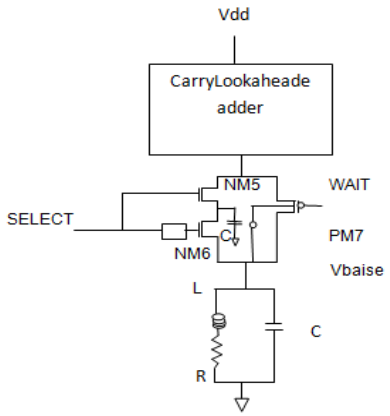

Figure.5. Modified Carry look ahead adder with Power Gating and ground bounce Noise

III. EXPERIMENTAL SETUP & SOFTWARE

We have used Empyrean Aether" tool at 180nm technology at various voltage and temperatures

IV. RESULTS AND ANALYSIS

In this section, we have performed simulation of our base structure Carry look ahead Adder and modified Carry ahead Adder (FBB Power Gating) on Empyrean Aether Tool at 180 nm Technology.

- **ACTIVE POWER**

  The Active power is dissipated by the circuit when the circuit is operation state. Here we will calculate the active power of circuit on the basis of voltage and temperature at 180 nm technology. The Active power includes both dynamics and static power. The Active power consumption of CMOS circuit [17] [18] is described by the following equation.

$$P_{active} = P_{dynamic} + P_{static} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (9)$$

$$P_{active} = P_{switch} + P_{short} + P_{leak} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (10)$$

$$P = \alpha_{0\to1} \times C_1 \times F_{clock} \times V_{dd}^2 + I_{short-circuit} \times V_{dd} + I_{leakage} \times V_{dd} \quad \ldots\ldots\ldots (11)$$

Where, α_{0-1} Probability, C_l=Load capacitance, F_c=Clock frequency, V_{dd}=Power supply, Ishort=Short circuit current, I_{Leak} Leakage current. As shown the table 4.3.in case of modified Carry look ahead adder with forward body biased Stacking Power Gating active power is reduced compared to base Carry look ahead adder. The reduction is almost 57.92 % at voltage 1.8 V and temperature 27 ^{o}C.

TABLE 1 ACTIVE POWER DISSIPATION OF CARRY LOOK AHEAD ADDER

Circuit	**Con. Carry Look Ahead Adder**		**Modified Carry Look**	
Supply and Temperature	1.8 V	27 ^{o}C	1.8 V	27 ^{o}C
Active power (nW)	3.58	3.58	1.35	1.35

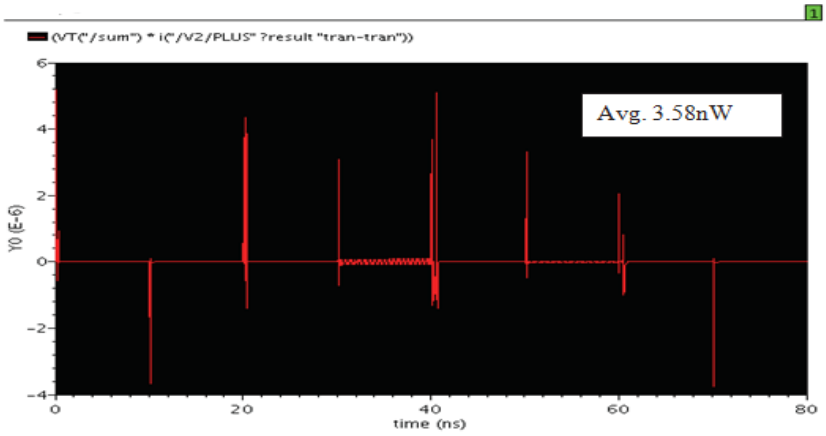

Figure 7 (a) Active power of conventional Carry Look Ahead Adder

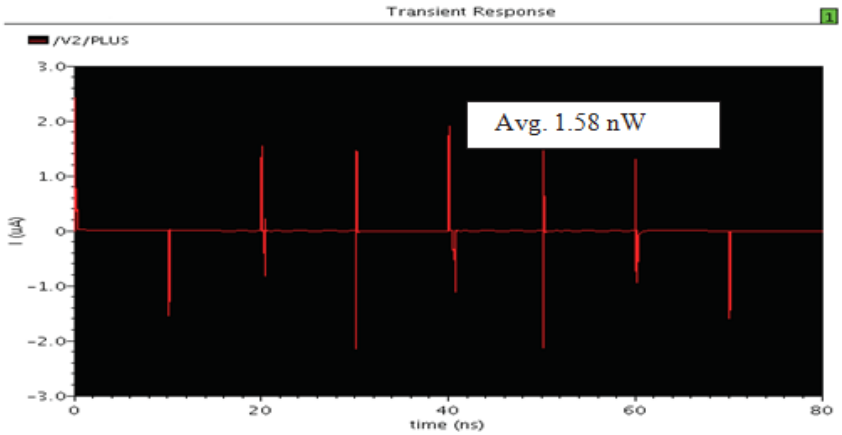

Figure 7 (b) Active power of modified Carry Look Ahead Adder

- **STANDBY LEAKAGE CURRENT**

The stand by leakage is obtained when the circuit in idle mode. Here we connect the sleep transistor to the pull down network of Carry look ahead adder circuit and ground of the circuit. When we measuring the leakage current in MTCMOS Power gating then the both transistors are off [18]. The basic equation of stand by leakage is

$$Leak = Isub + Iox \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (14)$$

Where, I_{sub} = Sub threshold leakage current, I_{ox} = Gate oxide current. Stand by leakage current is measured by at 1.8V and 27°C. It is greatly reduced almost 69% in modified Carry look ahead adder with Stacking Power Gating. The table 2 shows the leakage current at various voltages and various temperatures [20].

TABLE 2 (A) STANDBY LEAKAGE CURRENT AND LEAKAGE POWER DUE TO VARIOUS VOLTAGES

Volt. (V)	Leakage current		Leakage power	
	Conventional Carry look ahead (nA)	Modified Carry look ahead (pA)	Conventional Carry look ahead (mW)	Modified Carry look ahead (nW)
1.6	0.92	1.31	4.99	4.15
1.8	4.38	1.86	16.68	11.61
2.0	10.37	4.87	32.39	17.76
2.2	17.6	11.59	56.75	34.85
2.4	25.8	19.34	84.73	45.98

TABLE 2 (B) STANDBY LEAKAGE CURRENT AND LEAKAGE POWER DUE TO VARIOUS TEMPERATURES

Temp. ^0C	Leakage current		Leakage power	
	Conventional Carry look ahead adder (nA)	Modified Carry look ahead adder	Conventional Carry look ahead adder	Modified Carry look ahead adder (n W)
27	4.38	1.86	16.68	11.61
47	4.46	1.92	17.43	12.68
67	4.60	2.02	18.19	13.77
87	4.84	2.16	18.91	14.09
107	4.91	2.30	19.63	14.56

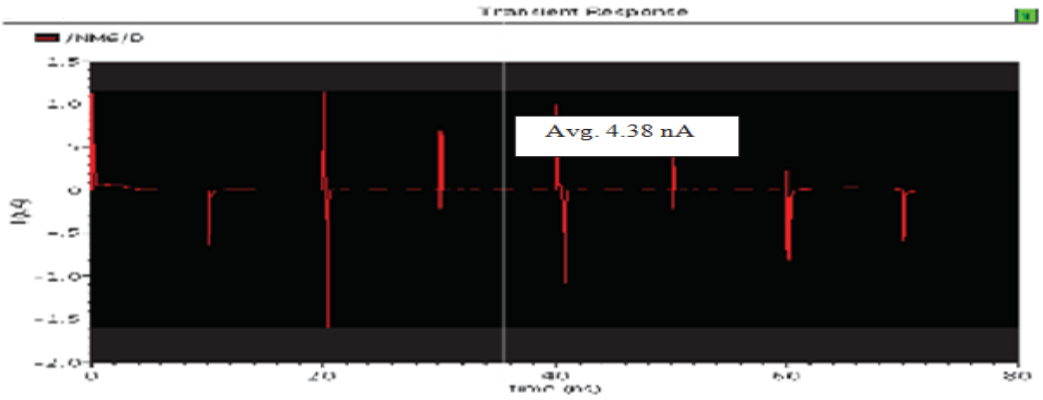

Figure 8 (a) Leakage current of conventional Carry Look Ahead Adder

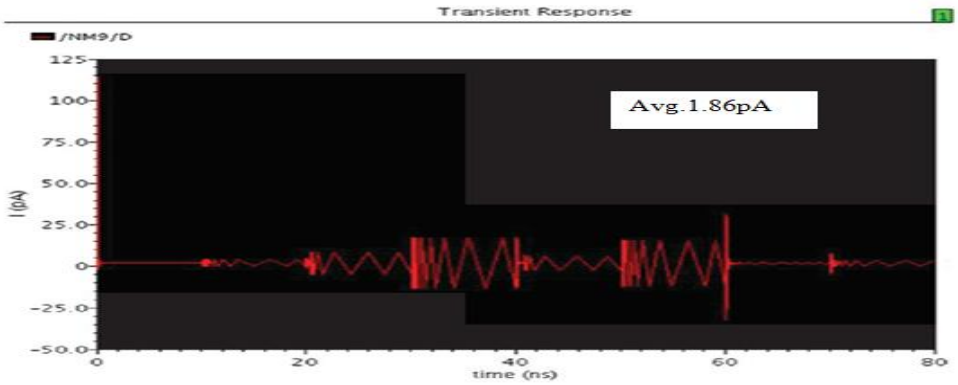

Figure 8 (b) Leakage current of modified Carry Look Ahead Adder

- **LEAKAGE POWER**

The stand by leakage power is measured at the time of idle mode. Here measured the leakage power when the sleep transistor is off. Basically the stand by leakage power is the product of the leakage current and supply voltage [19].The basic equation of leakage power is

$$Pleak = Ileak \cdot Vdd \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (15)$$

The Table 2 (a) and Table 2 (b) shows leakage power is reduced in various voltages and temperatures after applying stacking power gating.

- **GROUND BOUNCE NOISE**

During the active mode of the circuit an instant current pass from sleep transistor, which is saturation region and causes a sudden rush of the current. Elsewhere , because of self inductance of the off- chip bonding wires and parasitic inductance on chip power rails, result voltage function in the circuit depends on input/ output buffers and internal circuitry. The noise depends on the voltage. The ground bounce noise mode is in Fig 10. [20][21].

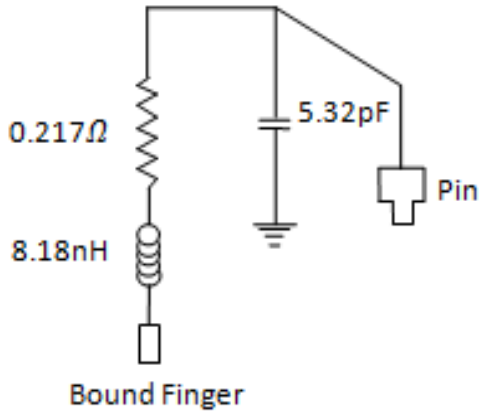

Figure.10: DIP-40 Package Pin Ground Bounce Noise mode

• Inductance L = 8.18 nH

• Resistance R = 0.217 Ω

• Capacitance C = 5.32 pF

The following wave form is showing ground bounce noise of conventional Carry look ahead Adder and modified Carry look ahead Adder.

TABLE 3.GROUND BOUNCE NOISE FOR CARRY LOOK AHEAD ADDER

Voltage (V)	Ground Bounce Noise (nV)		Temp ^{0}C	Ground Bounce Noise (nV)	
	Conv.	Modified		Conv	Modified
1.6	65.30	18.34	27	63.63	41.85
1.8	63.80	40.75	47	66.42	33.26
2.0	96.40	64.41	67	69.33	44.31
2.2	125.90	89.23	87	74.66	53.32
2.4	157.14	115.90	107	80.40	63.92

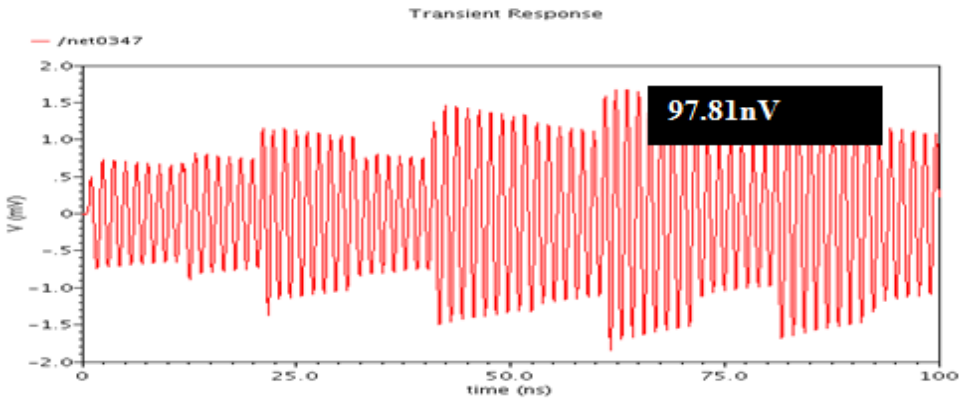

Figure 11 (a) Ground Bounce Noise of Conventional Carry look ahead Adder

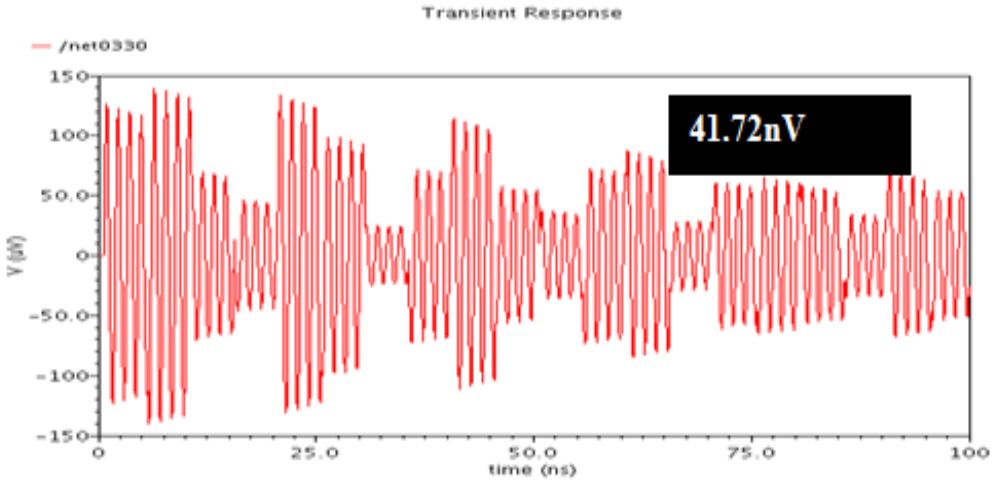

Figure 11.(b) Ground Bounce Noise of modified Carry look ahead Adder

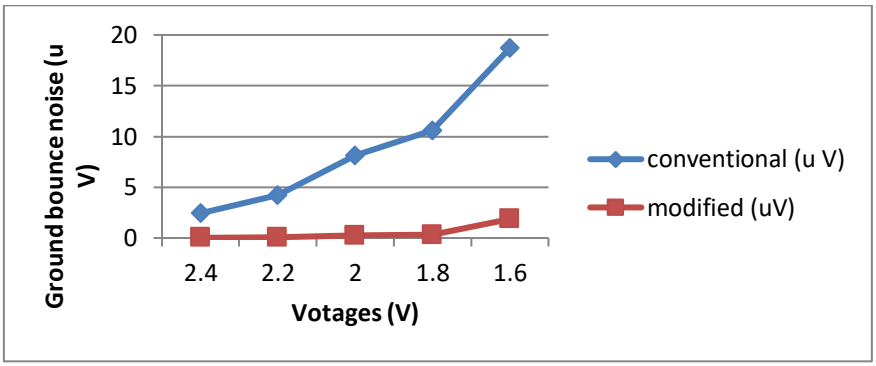

Figure 12. (a) Ground Bounce Noise graph of Carry look ahead Adder at various voltages

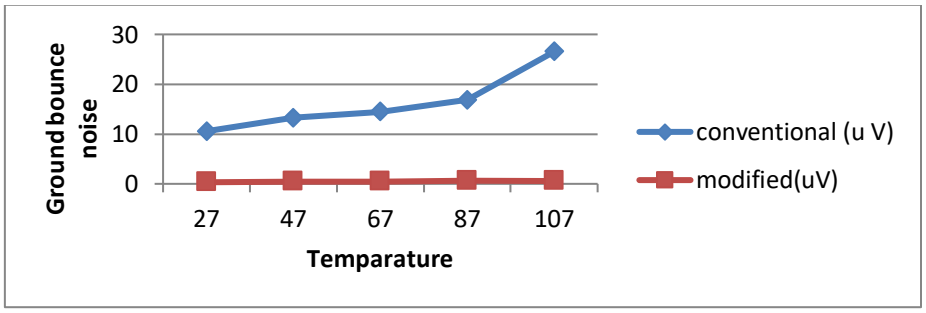

Figure 12 (b): Ground Bounce Noise graph of Carry look ahead Adder at various Temperatures

As shown in the table, the ground bounce noise is reduced up to 58% in to various voltage and temperature.[24]

V. CONCLUSION

In this paper we proposed a modified pass transistor based carry look ahead for microprocessor and arithmetic logic circuit with low ground bounce noise and reduced standby leakage current and leakage power[25]. Here we have used high performance power gating technique (forward body biased Stacking Power Gating Technique.) to reduced active power, leakage power, standby leakage current and ground bounce noise [26]. The leakage current is up to 42% and leakage power up to 69 %. The ground bounce noise is reduced to up to 58% and active power is reduced up to 37 %. The proposed modified Carry Look Ahead adder is operated at various voltages and various temperatures.

ACKNOWLEDGEMENT

I would like to thank my mentor Mr. Raghvendra Singh Assistant Professor for introducing me to this exciting area of New High Performance Low Power Carry Look Ahead Adder With Reduce Ground Bounce Noise Using MTCMOS Technique. . I would like to thank Dr. Vivek Srivastva Dean, Faculty of Engineering and Technology, for the valuable suggestions time to time. I would also like to thank Mr. Samir Mishra, Assistant Professor, HOD Electronics and Communication Engineering, for the valuable suggestions time to time in my programming & simulation work Authors would also like to Manish Kumar, Md. Anwar Husain, Sajal K.Paul thanks to This work is supported by Rama University Uttar Pradesh, Kanpur. for providing valuable suggestion in MTCMOS Technique.

REFERENCES

[1] Manish Kumar, Md. Anwar Hussain, Sajal K.Paul" An Improved SOI CMOS Technology Based Circuit Technique for Effective Reduction of Standby Sub threshold Leakage", S Scientific Research, Circuits and Systems, 2013, 4, 431-437.

[2] Radu Zlatanovici, Sean Kao, Borivoje Nikolic, "Energy-Delay of Optimization 64-Bit Carry-Lookahead Adders With a 240ps 90nm CMOS Design Example," IEEE J. Solid State circuits, vol.44, no. 2, pp. 569-583, Feb. 2009.

[3] K.Navi, O. Kavehei, M. Rouholamini, A. Sahafi, S. Mehrabi, N. Dadkhai, "Low-Power and High-Performance 1-bit CMOS Full Adder Cell," Journal of Computers, Academy Press, vol. 3, no. 2, Feb. 2008.

[4] Tripti Sharma, K.G. Sharma, Prof. B. P.Singh, "High Performance Full Adder Cell:Comparative Analysis", Proceedings of 2010 IEEE Students' Technology Symposium, IIT Kharagpur, 3-4 April 2010.

[5] Harmander Singh, Kanak Agarwal, Dennis Sylvester, Kevin J. Nowka, Enhanced Leakage Reduction Techniques Using Intermediate Strength Power Gating, "IEE Transactions on VLSI Systems

[6] ,Vol.15, No.11, November2007.

[7] Tripti Sharma, Prof.B.P.Singh, K.G.Sharma, Neha Arora Electronics & Communication Deptt. MITS Deemed University, Rajasthan INDIA, "High Speed, Low Power 8T Full Adder Cell with 45% Improvement in Threshold Loss Problem", Recent Advances in Networking, VLSI and Signal Processing.

[8] Mohammad Hossein Moaiyeri and Reza Faghih Mirzaee, Keivan Navi, "Two New Low-Power and High

[9] -Performance Full Adders", Journal Of Computers, Vol. 4, No. 2, February 2009.

[10] T. Vigneswaran, B. Mukundhan, and P. Subbarami Reddy, "A Novel Low Power, HighSpeed 14Transistor CMOS Full Adder Cell with 50% Improvement in Threshold Loss Problem", World Academy of Science, Engineering and Technology 13, 2008.

[11] R. Bhanuprakash, Manisha Pattanaik and S. S. Rajput, " Analysis and Reduction of Ground Bounce Noise and Leakage Current During Mode Transition of Stacking Power Gating Logic Circuits ",IEEE

[12] Region 10 Conference TENCON2009, pp. 1-6.

[13]

[14] Charbel J. Akl, Rafic A. Ayoubi, Magdy A. Bayoumi, "An effective staggered-phase damping technique for suppressing power-gating resonance noise during mode transition," 10th International Symposium on Qualityof Electronic Design, pp.116-119, 2009.

[15] Neil H. E. Weste, David Harris and Ayan Banerjee, "CMOS VLSI Design: A Circuit and System Perspective", Pearson Education, Third Edition 2011.

[16] Manisha Pattanaik, Muddala V. D. L. Varaprasad and Fazal Rahim Khan " Ground Bounce Noise Reduction of Low Leakage 1-bit Nano-CMOS based Full Adder Cells for Mobile Applications",

[17] International Conference on Electronic Devices, Systems and Applications (ICEDSA) 2010, pp. 31-36.

[18] Ku He, Rong Luo, Yu Wang, "A Power Gating Scheme for Ground Bounce Reduction During Mode Transition", 25th International Conference on Computer Design (ICCD) 2007, pp. 388-394.

[19] Yingtao Jiang, Abdulkarim Al-Sheraidah, Yuke Wang, Edwin Sha and Jin-Gung Chung, "Low Power Full Adder Using 8T Structure", IEEE Transactions on Circuits and Systems –II: Express Briefs, Vol.51, No.7, July 2004.