

Performance Techniques PV Neutra

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Abstract- This paper presents performance comparisons of different modulation techniques for Induction motor fed by cascaded Neutral-Point-Clamped Inverter (NPC). This paper provides a simple way to implement sinusoidal pulse-width modulation (PWM) and space vector pulse-width modulation (SVPWM) for cascaded Neutral-Point-Clamped Inverter (NPC). The output voltages and power of all inverter modules and the two series-capacitor dc voltages of each inverter module are perfectly balanced. The internal voltage drop of the inverter, due to the cascade structure of many insulated-gate bipolar transistor–diode modules’ series connection, is analyzed, which causes the distorted phase voltages and currents at low speeds when the frequency and the output voltage are low. The waveforms of rotor currents, rotor speed, electromagnetic torque, stator currents verify the proposed scheme.

Keywords- Cascaded multilevel (CML) Inverter, medium voltage (MV) drives, Sinusoidal Pulse-Width Modulation (PWM), Space Vector Pulse-Width Modulation (SVPWM).

I. INTRODUCTION

MEDIUM-VOLTAGE Adjustable-Speed-Drive (MV-ASD) systems offer significant advantages in a wide range of industrial applications such as fan, pump, and many improved process control systems with higher efficiencies combined with

energy savings. The induction-motor (IM) drives present an attractive solution because they are cheapest and rugged. One aspect of CML inverter apart from the three-level NPC inverter is to utilize small inverter bridges with relatively low voltage to synthesize and reach high voltage, thus, is more suitable for high-voltage, high-power applications [1]–[13]. Main drawback of cascaded H-bridge inverter is the need of excessive number of transformer windings. To alleviate this

problem, the cascaded NPC inverter was introduced and developed [14].

For the cascaded H-bridge and NPC inverters, a variety of modulation strategies have been reported, with the most popular being carrier-based pulse-width modulation (SPWM) [6], [15], [16], space-vector modulation (SVPWM) [17]–[22].

Another issue about the CML configuration is the internal voltage drop from the cascaded series connection of the insulated-gate bipolar transistor (IGBT)–diode modules, which becomes substantially high at low speeds when the output voltage is relatively low. The internal voltage drop causes severe voltage and current distortions at low speeds when the voltage is low.

IGBTs able to support a voltage of 6.5 kV are now available [2], [3]; however, the commutation speed of 6.5 kV IGBTs is rather lower than that of 3.3 kV IGBTs, available since some years. Therefore, in high-voltage converter it is still convenient to employ a Neutral Point Clamped (NPC) structure based on 3.3 kV IGBTs. NPC inverters halve the maximum drop voltage on their power devices because they are built up of four switches per phase, furnish a three-level voltage output and improve the current tracking performances in current control loops; moreover, they present a better harmonic content of the output current than traditional VSI, allowing a torque ripple reduction.

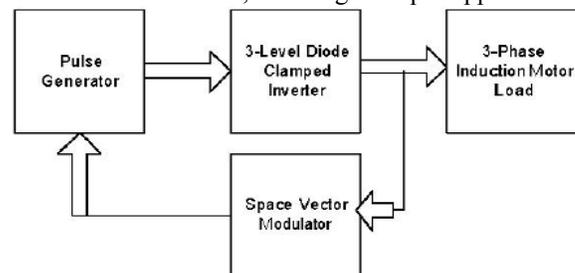


Fig. 1 Block Diagram induction motor fed by cascaded neutral-point-clamped inverter

II. CASCADED NEUTRAL-POINT-CLAMPED NPC INVERTER

One of the multilevel structures that has gained much attention and widely used is the Neutral-Point-Clamped multilevel inverter or also known as Diode Clamped multilevel

inverter. In case of 3-level NPC inverter, clamping diode, D1 and D4 clamped the DC bus voltage into three voltage level, $+v_{dc}/2$, 0 and $-v_{dc}/2$. The two series-capacitor voltages should be balanced during operation, namely, the average volt-ages across the two capacitors should be maintained the same, $v_{c1} = v_{c2}$. In addition, the voltage and power of all NPC modules must be well balanced.

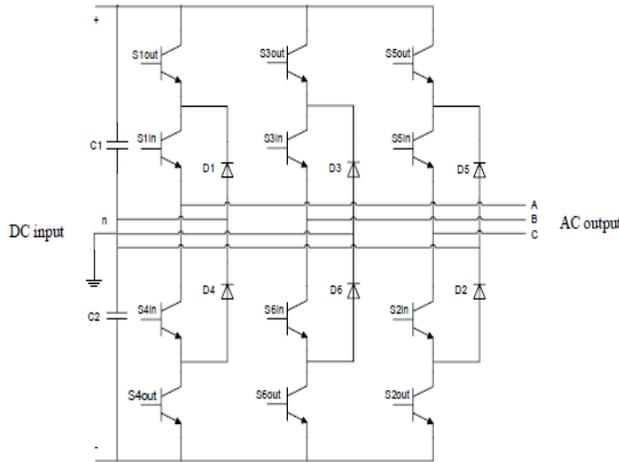


Fig. 2 3-level Neutral-point-Clamped inverter

III. MODULATION TECHNIQUES

As in 3-level NPC Inverter, modulation strategies can be framed into two main techniques:

- 1) Sinusoidal Pulse Width Modulation techniques;
- 2) Space Vector Modulation techniques
 - a) Open loop Control
 - b) Close loop Control

The first modulation techniques, widely used in industrial applications, are based on the comparison, separately for each inverter phase, between suitable analogical signals. Therefore, the commutation instants of the IGBT are determined by the comparators outputs, e.g. from the intersections of the signals applied to the comparators. SVM techniques, instead, determine the modulated waveforms taking into account simultaneously the desired voltage for all the inverter phases

A. SPWM Technique for Cascaded NPC Inverter

In general, the two carriers are selected in phase opposition (Fig. 3.a) or in phase (Fig. 3.b) between them. A comparison between the two solutions has shown that the choice of two carriers in phase provides a better harmonic content; therefore these will be afterwards used.

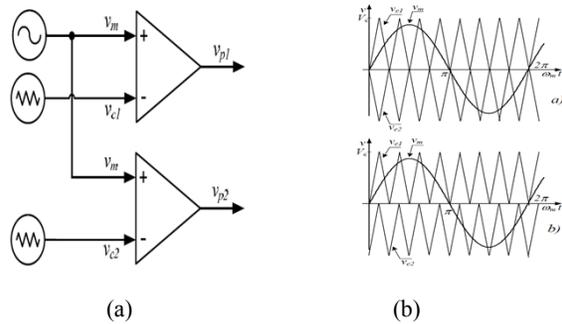


Fig. 3(a) Simulation of the modulating and the carrier signals

(b) Waveforms of the modulating and the carrier signals

B. SVPWM Technique for Cascaded NPC Inverter

1. Open Loop Control

Space Vector Modulation is a technique where the reference voltage is represented as a reference vector to be generated by the power converter. For the operation of 3-level inverter, there are 3 switching states for each inverter leg; [P], [O] and [N]. [P] denotes that the upper two switches in leg A are on and the inverter terminal voltage, V_{AN} is $+v_{dc}/2$, while [N] means that the lower two switches are on with a terminal voltage of $-v_{dc}/2$. Switching state [O] signifies that the inner two switches are on with the terminal voltage equals to zero. There are a total of 27 combination of switching states for NPC inverter.

The determination of switching instant may be achieved using space vector modulation technique based on the representation of switching vectors in α - β plane. The Space vector modulation technique is an advanced, computation intensive PWM technique and is possibly the best among all the PWM techniques for drives applications. Because of its superior performance characteristics, it is been finding wide spread application in recent years.

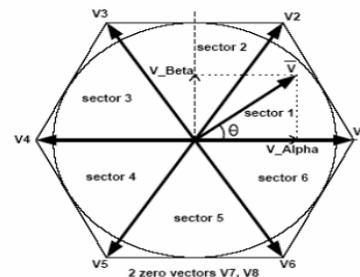


Fig. 4 Space Vector representation

i) Principle of Space Vector PWM

- Treats the sinusoidal voltage as a constant amplitude vector rotating at constant frequency.

- This PWM technique approximates the reference voltage v_{ref} by a combination of the eight switching patterns (v_0 to v_7).
- Coordinate Transformation (abc reference frame to the stationary $d-q$ frame):

A three-phase voltage vector is transformed into a vector in the stationary $d-q$ coordinate frame which represents the spatial vector sum of the three-phase voltage.

ii) Realization of Space Vector PWM

The space vector PWM is realized based on the following steps:

- Step1. Determine v_d, v_q, v_{ref} , and angle (α).
- Step2. Determine time duration T_o, T_1, T_2 .
- Step3. Determine the switching time of each switches.

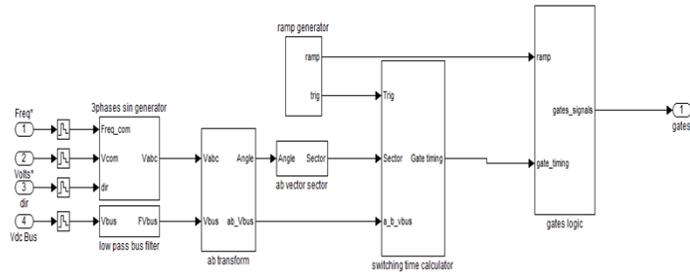


Fig. 5 Space-vector pulse-width modulation Gate pulse generation

2. Close Loop Control (Vector Control)

Fig. 6 shows the rotor-flux-oriented vector control for IM drives, where G_c is a speed regulator with the proportional and integral type. The current closed-loop control implements the current compensation to force the actual currents track the desired currents. ω_e and ω_s are respective synchronous and slip angular frequencies. ω_r^* and ω_r are desired and estimated rotor speed, respectively, and ω_r is calculated using the back-EMF-based model reference adaptive system (MRAS) speed estimation in [31]. A_r, d_r, i_r, d_s and i_r, q_s denote the d -axis component of the rotor-flux-linkage vector and the dq -axis components of the stator-current vector, in the rotor-flux frame, respectively. i_α^* and i_β^* are $\alpha\beta$ -axis components of the stator current vector in stator frame, and the superscript symbol “*”

denotes the desired value. i_a, i_b And i_c are three phase currents, and v_a, v_b, v_c are three phase voltages. T_e denotes the motor torque.

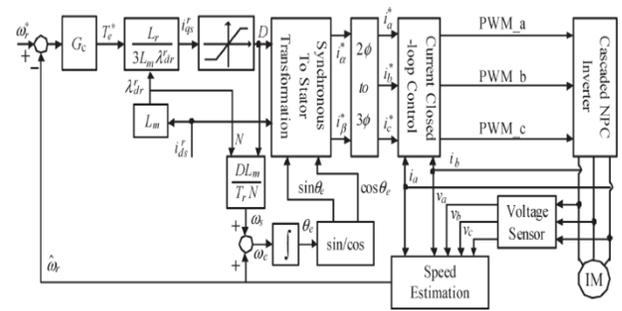


Fig. 6 Speed-sensing vector-control based IM drive

IV. SIMULATION RESULTS AND DISCUSSIONS

The simulation tests were performed taking into account a Field Oriented Controlled drive employing an cascaded NPC inverter, supplied by a 800V DC link and Induction motor of rating 5HP, 460V, 60Hz, 1778 rpm at different torque input.

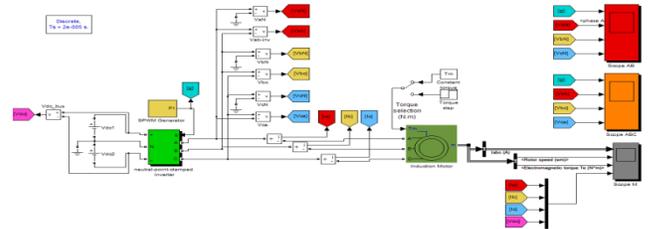


Fig. 7 Simulation model of NPC fed by SPWM

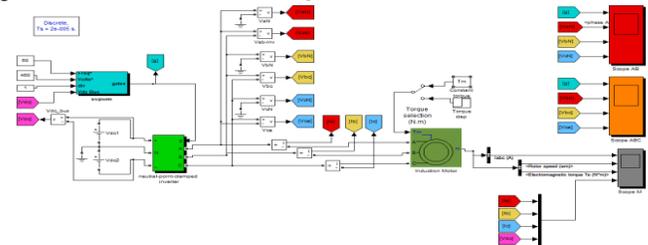


Fig. 8 Simulation model of NPC fed by SVPWM

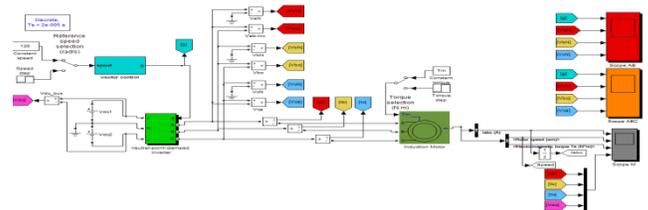


Fig. 9 Simulation model of NPC fed by SSSVC

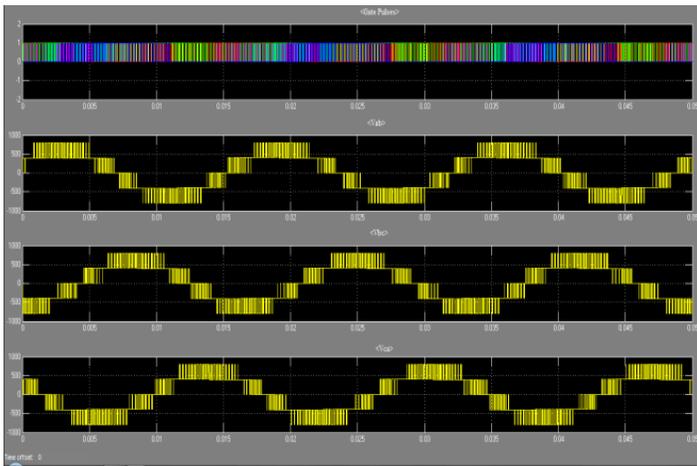


Fig. 10 Waveform of Gate pulses and line voltages of SPWM

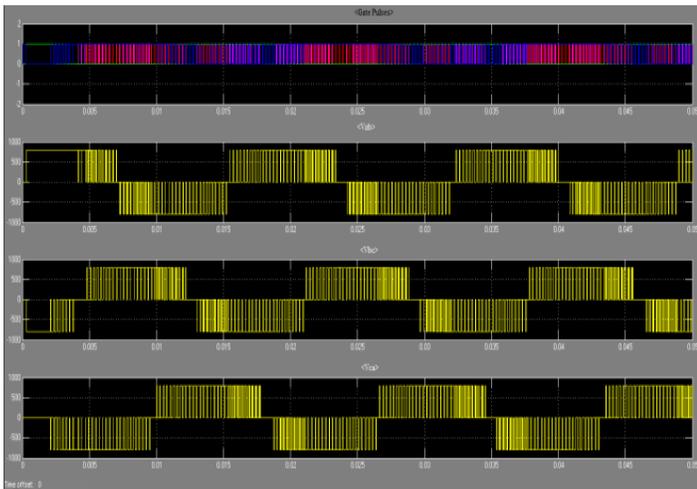


Fig. 11 Waveform of Gate pulses and line voltages of SVPWM

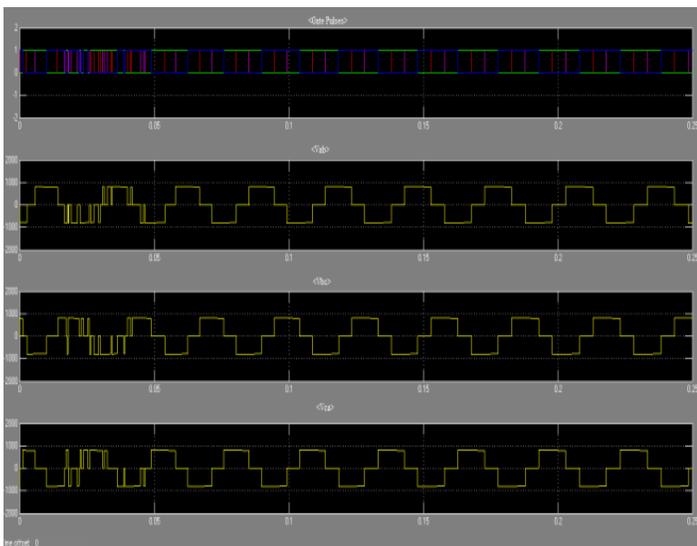


Fig. 12 Waveform of Gate pulses and line voltages of SSVC

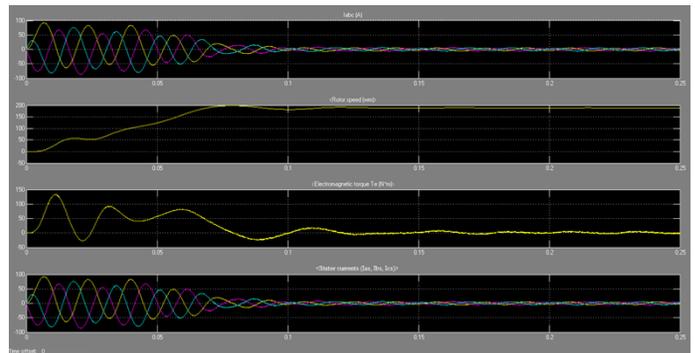


Fig. 13 Waveforms of rotor currents, speed, torque, stator currents of SPWM

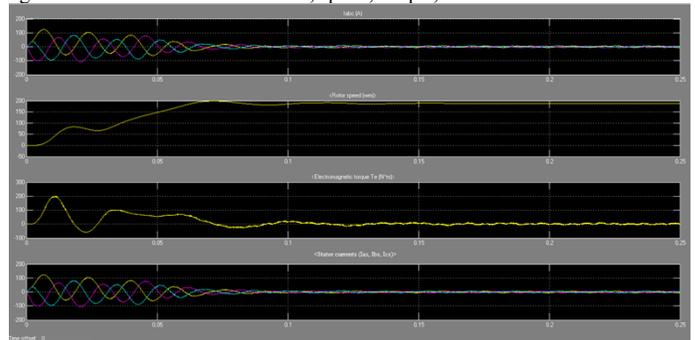


Fig. 14 Waveforms of rotor currents, speed, torque, stator currents of SVPWM

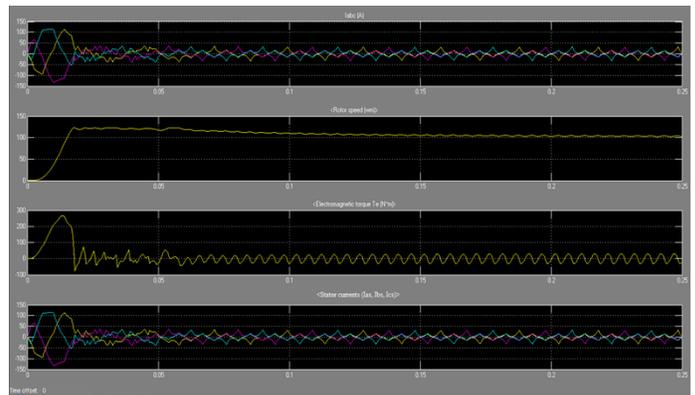


Fig. 15 Waveforms of rotor currents, speed, torque, stator currents of SSVC

V. COMPARISON BETWEEN SPWM AND SVPWM

The performances of the proposed modulation technique have been compared. The simulation tests were performed taking into account a Field Oriented Controlled drive employing an NPC inverter, the first comparison has been carried out considering the drive during the steady-state with an applied load torque equal to the rated one. The reference speed has been selected so that the supply frequency is about equal to 60 Hz. The table points out a remarkable difference between the distortions introduced by the two modulation techniques. In fact

the Total Harmonic Distortion (THD %) produced by the SPWM is equal to 2.44, while that introduced by the SVM is equal to 2.10. Settling time of motor verify the comparison of modulating techniques.

TABLE I
COMPARISON OF LOAD CURRENT THD

Load currents (A)	SPWM (THD %)	SVPWM (THD %)	SSVC (THD %)
I	2.44	2.10	1.90

TABLE II
COMPARISON OF SETTTLING TIME (Ts) IN SEC

Torque (T_m) N-m	SPWM (Ts) Sec	SVPWM (Ts) Sec	SSVC (Ts) Sec
0	0.12	0.10	0.05
5	0.15	0.12	0.75
10	0.17	0.15	0.80

VI. CONCLUSIONS

This paper describes three different modulation techniques, suitable for NPC inverters supplying an induction motor, and exhibits a comparison between them, taking into account the harmonics introduced on the motor stator current. Second modulation technique is a Space Vector Modulation, proposed by the authors, specific for NPC inverters. The main peculiarity of the proposed SVM consists on performing, in every operating condition, only one commutation per phase during each sampling period. The comparison has shown that the proposed SVM always produces a smaller harmonic distortion; besides, it presents a lesser limitation on the maximum value of the output voltage module than the SPWM.

REFERENCES

[01] G.Mondal, K. Sivakumar, R. Ramchand, K. Gopakumar, and E. Levi, "A dual seven-level inverter supply for an open-end winding induction motor drive," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1665–1673, May 2009.

[02] M. A. Perez, P. Cortes, and J. Rodriguez, "Predictive control algorithm technique for multilevel asymmetric cascaded H-bridge inverters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 12, pp. 4354–4361, Dec. 2008.

[03] P. Lezana, J. Rodriguez, and D. A. Oyarzun, "Cascaded multilevel inverter with regeneration capability and reduced number of switches," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1059–1066, Mar. 2008.

[04] D. Krug, S. Bernet, S. S. Fazel, K. Jalili, and M. Malinowski, "Comparison of 2.3-kV medium-voltage multilevel converters for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2979–2992, Dec. 2007.

[05] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[06] L. M. Tolbert, F. Z. Peng, T. Cunnyngham, and J. N. Chiasson, "Charge balance control schemes for cascade multilevel converter in hybrid electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1058–1064, Oct. 2002.

[07] O. Lopez, J. Alvarez, J. Doval-Gandoy, and F. D. Freijedo, "Multilevel multiphase space vector PWM algorithm," *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 1933–1942, May 2008.

[08] M. Rotella, G. Penailillo, J. Pereda, and J. Dixon, "PWM method to eliminate power sources in a non redundant 27-level inverter for machine drive applications," *IEEE Trans. Ind. Electron.*, vol. 56, no. 1, pp. 194–201, Jan. 2009.

[09] J. I. Leon, R. Portillo, S. Vazquez, J. J. Padilla, L. G. Franquelo, and J. M. Carrasco, "Simple unified approach to develop a time-domain modulation strategy for single-phase multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 9, pp. 3239–3248, Sep. 2008.

[10] P. W. Hammond, "Enhancing the reliability of modular medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 948–954, Oct. 2002.

[11] J. I. Leon, S. Vazquez, A. J. Watson, L. G. Franquelo, P. W. Wheeler, and J. M. Carrasco, "Feed-forward space vector modulation for single-phase multilevel cascaded converters with any DC voltage ratio," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 315–325, Feb. 2009.

[12] Y. Cheng, C. Qian, M. L. Crow, S. Pekarek, and S. Atcity, "A comparison of diode-clamped and cascaded multilevel converters for a STATCOM with energy storage," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1512–1521, Oct. 2006.

[13] J. A. Barrera, L. Marroyo, M. A. R. Vidal, and J. R. T. Apraiz, "Individual voltage balancing strategy for PWM cascaded H-bridge converter based STATCOM," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 21–29, Jan. 2008.

[14] A. Joseph, J. Wang, Z. Pan, L. Chen, and F. Z. Peng, "A 24-pulse rectifier cascaded multilevel inverter with minimum number of transformer windings," in *Conf. Rec. 40th IEEE Ind. Appl. Soc. Annu. Meeting*, Oct. 2005, vol. 1, pp. 115–120.

[15] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, P. Ibanez, and J. L. Villate, "A comprehensive study of a hybrid modulation technique for the neutral-point-clamped converter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 294–304, Feb. 2009.

[16] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858–867, Aug. 2002.

[17] B. P. McGrath, D. G. Holmes, and T. A. Lipo, "Optimized space vector switching sequences for multi-level inverters," in *Proc. IEEE Appl. Power. Electron. Conf. 16th Annu. Meeting, Anaheim, CA*, Mar. 2001, vol. 2, pp. 1123–1129.

[18] R. S. Kanchan, M. R. Baiju, K. K. Mohapatra, P. P. Ouseph, and K. Gopakumar, "Space vector PWM signal generation for multilevel inverters using only the sampled amplitudes of reference phase voltages," *Proc. Inst. Elect. Eng.—Elect. Power Appl.*, vol. 152, no. 2, pp. 297–309, Mar. 2005.

[19] M. A. S. Aneesh, A. Gopinath, and M. R. Baiju, "A simple space vector PWM generation scheme for any general n-level inverter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1649–1656, May 2009.

[20] A. Gopinath, M. A. S. Aneesh, and M. R. Baiju, "Fractal based space vector PWM for multilevel inverters—a novel approach," *IEEE Trans. Ind. Electron.*, vol. 56, no. 4, pp. 1230–1237, Apr. 2009.

[21] M. Saedifard, R. Iravani, and J. Pou, "A space vector modulation strategy for a back-to-back five-level HVDC converter system," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 452–466, Feb. 2009.

[22] J. I. Leon, S. Vazquez, R. Portillo, L. G. Franquelo, J. M. Carrasco, P. W. Wheeler, and A. J. Watson, "Three-dimensional feed forward

- space vector modulation applied to multilevel diode-clamped converters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 1, pp. 101–109, Jan. 2009.
- [23] Y. Liu, H. Hong, and A. Q. Huang, "Real-time calculation of switching angles minimizing THD for multilevel inverters with step modulation," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 285–293, Feb. 2009.
- [24] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWM method: A theoretical analysis," *IEEE Trans. Power Electron.*, vol. 7, no. 3, pp. 497–505, Jul. 1992.
- [25] J. Holtz and N. Oikonomou, "Neutral point potential balancing algorithm at low modulation index for three-level inverter medium voltage drives," *IEEE Trans. Ind. Appl.*, vol. 43, no. 3, pp. 761–768, May 2007.
- [26] A. Videt, P. L. Moigne, N. Idir, P. Baudesson, and X. Cimetiere, "A new carrier-based PWM providing common-mode-current reduction and DC-bus balancing for three-level inverters," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3001–3011, Dec. 2007.
- [27] H. du Toit Mouton, "Natural balancing of three-level neutral-point-clamped PWM inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1017–1025, Oct. 2002.
- [28] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, C. Jaen, and M. Corbalan, "Voltage-balance compensator for a carrier-based modulation in the neutral-point-clamped converter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 305–314, Feb. 2009.
- [29] R. Gupta, A. Ghosh, and A. Joshi, "Switching characterization of cascaded multilevel-inverter-controlled systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1047–1058, Mar. 2008.
- [30] B. P. McGrath, T. Meynard, G. Gateau, and D. G. Holmes, "Optimal modulation of flying capacitor and stacked multi cell converters using a state machine decoder," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 508–516, Mar. 2007.
- [31] F. Z. Peng and T. Fukao, "Robust speed identification for speed-sensor less vector control of induction motors," *IEEE Trans. Ind. Appl.*, vol. 30, no. 5, pp. 1234–1240, Sep. 1994.
- [32] H. W. v. d. Brocker, H. C. Skudenly, and G. Stanke, "Analysis and realization of a pulse width modulator based on the voltage space vectors," in *Conf. Rec. IEEE-IAS Annu. Meeting, Denver, CO*, pp. 244–251, 1986.
- [33] O. Ogasawara, H. Akagi, and A. Nabel, "A novel PWM scheme of voltage source inverters based on space vector theory," in *Proc. EPE European Conf. Power Electronics and Applications*, pp. 1197–1202, 1989.
- [34] D. Jenni and F. Wueest, "The optimization parameters of space vector modulation," in *Proc. 5th European Conf. Power Electronics and Applications*, pp. 376–381, 1993.
- [35] S. R. Bowes and Y. S. Lai, "The relationship between space vector modulation and regular-sampled PWM," *IEEE Trans. Power Electron.*, vol. 14, pp. 670–679, Sept. 1997.
- [36] J.-H. Youm and B.-H. Kwon, "An effective software implementation of the space-vector modulation," *IEEE Trans. Ind. Electron.*, vol. 46, pp. 866–868, Aug. 1999.
- [37] Zhou and D. Wang, "Relationship between space-vector modulation and three-phase carrier-based PWM: A comprehensive analysis," *IEEE Trans. Ind. Electron.*, vol. 49, pp. 186–196, Feb. 2002.
- [38] E. Levi, R. Bojoi, F. Profumo, H. A. Toliyat, S. Williamson, "Multiphase induction motor drives – a technology status review," *IET Electric Power Applications*, vol. 1, no. 4, pp. 489–516, 2007.
- [39] E. Levi, "Multiphase electric machines for variable-speed applications," *IEEE Trans. on Industrial Electronics*, vol. 55, no. 5, pp. 1893–1909, 2008.
- [40] B. Wu, "High-power converters and AC drives," IEEE Press - John Wiley & Sons, Hoboken, NJ, 2006.
- [41] J. Rodríguez, J. S. Lai, F. Z. Peng, "Multilevel inverters: A survey of topologies, controls and applications," *IEEE Trans. on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, 2002.
- [42] applications of multilevel converters," *IEEE Trans. on Industrial Electronics*, vol. 57, no. 8, pp. 2553–2580, 2010.