Effects of Scaling on Double-Gate Si-Nanowire Transistor

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Abstract – In this work we study the scaling effects on double gate Si Nanowire transistor. For it we use software which is based on a semi-classical approach. This model is implemented into surface potential so it is also called as surface potential based model. It shows excellent agreement with numerical simulations. The double-gate silicon nano transistor is better than the conventional MOSFET in terms of performance and behaviour.

Index Terms – Scaling, Quantum mechanics effects (QMEs), Rectangular nanowire gate-all-around (GAA) MOSFET, Short channel effects (SCEs), Compact modelling.

I. INTRODUCTION

Since Moore's law is not more effective now for need of semiconductor, dimensions are approaching the limit due to the increase the short channel effects (SGEs). Nanowire transistors have generated much research interest lately [1,2] confinement effects. They identified a size [3] because of their potential to replace the conventional planar structure in scaling CMOS devices to 10 nm gate length or below. It is difficult to scale bulk MOSFETs with acceptable short channel effect (SCEs) to below 20 nm.[4] These unwanted effects increase leakage currents so new device architectures such as multiple gates MOSFETs are becoming intense subjects of research. Multiple gate MOSFETs represent a good alternative to get better gate controllability.[5] The gate is used as a control terminal to switch on or off a current conduction channel between the source and drain terminals in a MOSFET. The channel region underneath the gate moderately doped. The source and drain regions are heavily doped to from n-p or p-n junctions to the oppositely doped structure. The simplest transistor scaling consists reducing the horizontal and vertical dimensions as well as the supply voltage, by the same factor in an attempt to keep the electric field in the scaled MOSFET. So, the real scaling implementations have been based on a little modified approach where the geometry and voltage are reduced by different factors, it is known as generalized scaling.

In this paper, we discuss the scaling effects on double- gate MOSFET with Drift-Diffusion models.

II. DRIFT DIFFUSION MODEL

The popular drift-diffusion current equations can be easily derived from the Boltzmann

transport equation by considering moments of the BTE. Consider steady state conditions and, for simplicity, a 1-D geometry. With the use of a relaxation time approximation, the Boltzmann transport equation may be written

$$\frac{eE}{m^*}\frac{\partial f}{\partial v} + v\frac{\partial f}{\partial x} = \frac{f_0 - f(v,x)}{\tau} \quad \text{..... (1.0)}$$

respect to their respective quantum

In writing Eq. (1.0) parabolic bands have been assumed for simplicity, and the charge *e* has to be taken with the proper sign of the particle (positive for holes and negative for electrons). The general definition of current density is repeated here for completeness

$$J(x) = e\int v f(v,x)dv \quad \text{..... (2.0)}$$

Where the integral on the right hand side represents the first 'moment' of the distribution function. After solving the equation the resulting drift-diffusion current expressions for electrons and holes are

$$Jn = qn(x)\mu_n E(x) + qD_n \frac{d_n}{dx}$$
$$Jp = qp(x)\mu_p E(x) + qD_p \frac{d_p}{dx} \quad \text{..... (3.0)}$$

respectively, where q is used to indicate the absolute value of the electronic charge. Although no direct assumptions on the non-equilibrium distribution function, $f(v,x)$, were made in the derivation of Eqs. (3.0), in effect, the choice of equilibrium (thermal) velocity means that the drift-diffusion equations are only valid for small perturbations of the equilibrium state (low fields). The validity of the drift-diffusion equations is empirically extended by introducing field dependent mobility $\mu(E)$ and diffusion coefficient $D(\mathbf{E})$, obtained from empirical models or detailed calculation to capture effects such as velocity saturation at high electric fields due to hot carrier effects.

The most common scaling factors for normalization of semiconductor equations are listed in Table-1

Table-1 : Scaling factors

Variable	Scaling variable	Formula
Space	Intrinsic Debye length (N=ni) Extrinsic Debye length (N=$Nmax$)	$L = \sqrt{\frac{\varepsilon K_g T}{q^2 N}}$
Potential	Thermal voltage	$V^* = \frac{K_B T}{q}$
Carrier concentration	Intrinsic concentration Maximum doping concentration	$N = n_i$ $N = N_{\max}$
Diffusion coefficient	Practical unit Maximum diffusion coefficient	$D = 1\frac{cm^2}{s}$ $D = D_{\max}$
Mobility		$M = \frac{D}{V^*}$
Generation-Recombination		$R = \frac{DN}{L^2}$
Time		$T = \frac{L^2}{D}$

III. SIMULATION

The fabrication of a multi-gate silicon nano transistor cannot be possible in our country due to some limitations such as temperature, clean room and other reasons. So for simulation of multi-gate nano transistor we use MUGFET simulator which creates the appropriate conditions for testing the result of it with different dimensions. The result of this simulator is approximately same as the original conditions. Simulation parameters for double-gate silicon nano transistor in detail shown in table – 2. According to the table we have drawn different curves between various parameters for double-gate silicon nano transistor.

Table–2 : Different parameters for simulation

Parameter	***Value***
Gate Metal/Al	$\phi \cong 4.8$
Gate length	30 nm
Drain length	6 nm
t_{ox}	2 nm
Source to Drain length	10 nm
Source to Drain doping	$10^{20} / cm^3$
Channel doping	$10^{15} / cm^3$

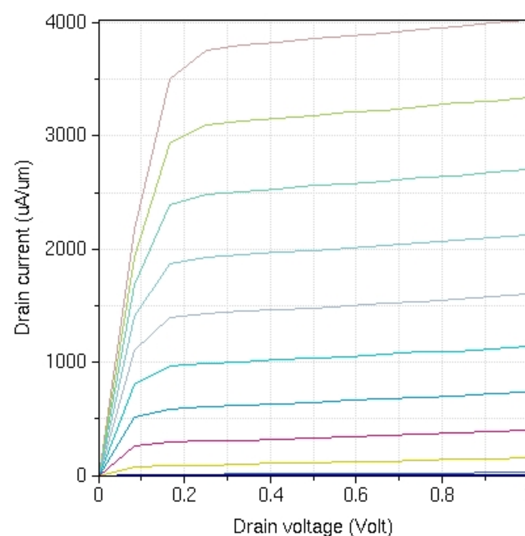

Fig – 1 : Drain current versus drain voltage curve

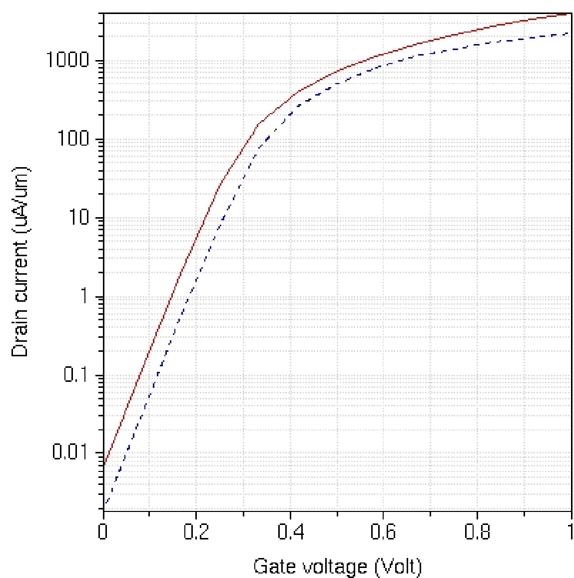

Fig – 2 : Drain current versus gate voltage curve

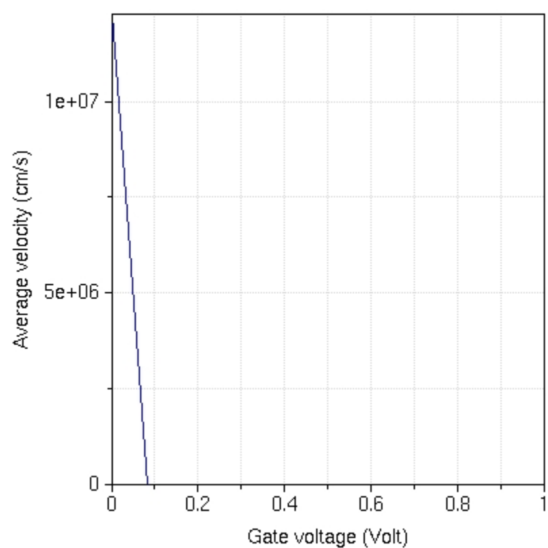

Fig – 3: Average velocity versus gate voltage curve

The curve between drain current and drain voltage for double-gate silicon nano transistor shows in figure – 1. At low drain voltage curve like linear but after 0.1 V its shows likely straight curve at different values of drain current. This curve show different drain current at various gate voltages. Figure - 2 curve represents drain current linearly increasing with gate voltage approximately 0.3 Volt, but after it increase slightly straight with 0.3 to 1 Volt value of gate voltage. Drain current drawn at low and high voltages in this curve. Both curves have minor difference only at high gate voltage. Curve in figure – 3 represents minor change in gate voltage with increasing the average velocity for wide range. We also say there is no highly variations in gate voltage.

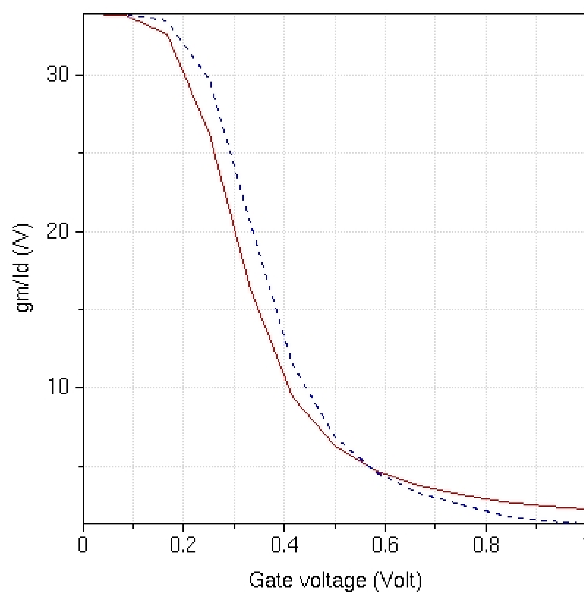

Fig. 4 : Transconductance/drain current versus gate voltage curve

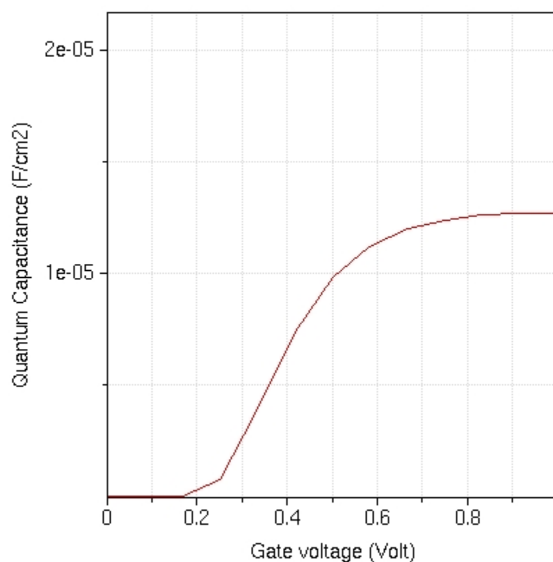

Fig . 5 : Quantum capacitance versus gate voltage curve

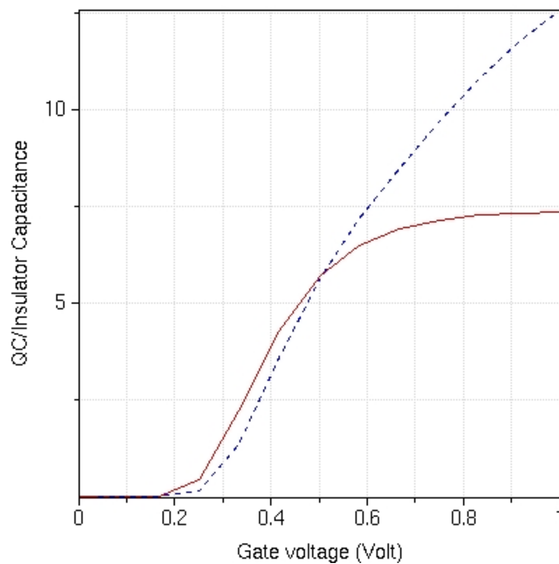

Fig – 6 : Quantum capacitance/insulator capacitance versus gate voltage curve

At low gate voltage gm/Id value is very high but after increasing the gate voltage gm/Id value decreasing slowly up to zero, which can be seen clearly in figure- 4. According to curve in figure – 5, quantum capacitance quickly increases with gate voltage range (0.275-0.5 V) and after this quantum capacitance increase slowly with gate voltage. Quantum capacitance quickly increase with gate voltage range (0.275-0.5 V) and after this quantum capacitance increase slowly with gate voltage but insulator capacitance increase linearly with gate voltage which shown in figure -6.

IV. CONCLUSION

In conclusion, the scaling of silicon nano transistors affects different parameters of multi-gate nano transistors. In this paper various curves have shown for double-gate silicon nano transistor. These scaling effects reduction in Ioff, undoped channel eliminates intrinsic parameter fluctuations, minimise impurity scattering, higher current drive capability and better control of short channel effects.

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